Hardness Assurance Testing and Radiation Hardening by Design Techniques for Silicon-Germanium Heterojunction Bipolar Transistors and Digital Logic Circuits

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

Hydrocarbon exploration, global navigation satellite systems, computed tomography, and aircraft avionics are just a few examples of applications that require system operation at an ambient temperature, pressure, or radiation level outside the range covered by military specifications. The electronics employed in these applications are known as "extreme environment electronics." On account of the increased cost resulting from both process modifications and the use of exotic substrate materials, only a handful of semiconductor foundries have specialized in the production of extreme environment electronics. Protection of these electronic systems in an extreme environment may be attained by encapsulating sensitive circuits in a controlled environment, which provides isolation from the hostile ambient, often at a significant cost and performance penalty. In a significant departure from this traditional approach, system designers have begun to use commercial off-the-shelf technology platforms with built in mitigation techniques for extreme environment applications. Such an approach simultaneously leverages the state of the art in technology performance with significant savings in project cost.

Silicon-germanium is one such commercial technology platform that demonstrates potential for deployment into extreme environment applications as a result of its excellent performance at cryogenic temperatures, remarkable tolerance to radiation-induced degradation, and monolithic integration with silicon-based manufacturing. In this dissertation the radiation response of silicon-germanium technology is investigated, and novel transistor-level layout-based techniques are implemented to improve the radiation tolerance of HBT digital logic.

CHAPTER 1

INTRODUCTION

1.1 Motivation

The electronic components that are used in extreme environments are exposed to high levels of radiation and wide temperature swings. Components that have undergone a verification procedure to ensure reliable operation under these conditions are known as "radiation-hardened" or "rad-hard." The "hardening" process typically involves a combination of innovative hardware and software solutions. Data redundancy, error-correction codes, and accurate environment models are all software-based solutions, while protective shielding, temperature control, and "radiation hardening by process" (RHBP) are hardware-based solutions. The term RHBP refers to any process deviation from the standard fabrication sequence that is done with the sole purpose of achieving an increase in the radiation tolerance of the technology platform. High-resistivity and silicon-on-insulator (SOI) substrates are two popular examples of RHBP solutions. Although RHBP is an effective approach in the mitigation of radiation-induced degradation, it commands such an extremely small share of the total microelectronics market because of the fact that rad-hard foundries have to contend with low yields, process instabilities, and high manufacturing costs. All of these challenges result in RHBP technology platforms that lag behind the state of the art commercial offerings by two to three technology generations. Moreover, the inability to overcome these challenges has proven detrimental to the RHBP electronics sector, as evidenced by the reduction in the number of rad-hard foundries from over 18 in 1985 [1] to just two, BAE [2] and Honeywell [3], in 2005. Meanwhile, the technology scaling pursued in accordance with Moore's Law has resulted in a paralleled, yet unintentional, increase in the radiation tolerance of many commercial process offerings.

The improvement in the radiation tolerance of these "commercial off-the-shelf" (COTS) electronics with increased scaling can be taken advantage of through innovative transistor

and circuit design techniques without sacrificing either performance or cost. This mitigation technique is known as "radiation hardening by design" (RHBD) and has been successfully implemented in COTS electronics as a viable alternative to the RHBP approach [4][5]. Investigations into RHBD solutions have traditionally targeted CMOS technology platforms since they dominate the IC market because of the sheer market volume of digital base-band electronics that require fast switching speeds and low power consumption. Without discounting the importance of CMOS, it must be emphasized much of the recent growth in global information traffic has been driven by data transmission over wireless links, which necessarily involves the design of analog and microwave circuits that use bipolar junction transistors (BJTs). BJTs are incorporated into these circuits to achieve high linearity, low $1/f$ noise, increased bandwidth, high output conductance, and large power gain. Moreover, in a true mixed-signal environment, a system-on-chip (SoC) solution is highly desirable since it reduces packaging complexity, parasitics, size, and system cost. *Silicon-Germanium* (SiGe) *Bipolar-CMOS* (BiCMOS) technology is capable of delivering such a solution by providing performance characteristics comparable to those of III-V material systems in an integrated silicon (Si) manufacturing environment with low cost and high yield [6]. It is therefore highly desirable to study the radiation response of SiGe BiCMOS technology platforms.

1.2 Organization of the Dissertation

The radiation response of SiGe HBTs and the impact of transistor-level layout-based RHBD techniques applied to HBT digital logic are investigated in this dissertation. These tasks are divided into three sections distributed over ten chapters. In the first section (Chapter 2), the relevant background material on the effects of radiation in microelectronic devices and circuits is presented. Chapter 2 begins with definitions of several parameters that are used in the measurement of radiation effects. This is followed by a literature review of the physical mechanisms underlying the observed radiation-induced degradation in microelectronics. Next, a description of the classical extreme environments relevant to this work is provided, and the chapter is concluded with a survey of the ground-based testing

facilities that are used to obtain data and an introduction to the SiGe BiCMOS technology platforms under investigation.

The second section (Chapters 3-6) deals primarily with the "Hardness Assurance Testing" component of the title by investigating the effects of atomic displacement and ionization in SiGe HBTs and proton- and heavy-ion-induced single-event effects in HBT digital logic. The impact of technology scaling on the response of SiGe HBTs to medium-energy proton irradiation is presented in Chapter 3 using a combination of *dc*- and ac-figures of merit, avalanche multiplication, neutral base recombination, mixed-mode stress, low-frequency noise, bias dependence, and high-temperature annealing. In Chapter 4, the effect of the particular radiation environment on the observed degradation is discussed with particular emphasis on the proton energy, irradiation source, dose rate, and ambient temperature. In Chapter 5, an analysis of the local sensitive areas in HBT digital logic, configured using a variety of circuit-based RHBD techniques, is presented using the results from single-photon pulsed laser irradiation of 128-bit shift registers. In Chapter 6, the impact of temperature on the single-event upset rate of HBT digital logic is investigated by comparing the response of 16-bit shift registers irradiated using a medium-energy proton broadbeam at room temperature to the response in a liquid nitrogen environment.

In the third section (Chapters 7-9), the "Radiation Hardening By Design" component of the title is addressed through the proposition of a layout-based RHBD implementation of the SiGe HBT. In Chapter 7, several variants of this RHBD approach are presented, and the optimal design amongst them is identified using a combination of heavy-ion microbeam irradiation and 3-D TCAD ion-strike simulations. In Chapter 8, two-photon pulsed laser irradiation is used to verify the efficacy of the RHBD design selected in Chapter 7, and a circuit-level demonstration of the single-event upset mitigation afforded using this RHBD technique is presented in Chapter 9.

The dissertation is concluded in Chapter 10 with the appropriate conclusions and recommendations for future work.

1.3 Contributions

The major contributions to the field of radiation effects in microelectronics made by this dissertation are listed below.

- Evaluation of the impact of technology scaling on the radiation response of 1st- through 4th-generation SiGe HBTs [7][8].
- Evaluation of the impact of source environment on the radiation response of 1st- through 4th-generation SiGe HBTs [9][10][11].
- Evaluation of circuit-level RHBD techniques for 1st-generation HBT digital logic [12].
- **First ever** demonstration of the enhanced susceptibility of HBT digital logic to single-event effects at cryogenic temperatures [13].
- Demonstration of a transistor-level layout-based technique for RHBD mitigation in 3rd-generation HBT digital logic [14][15].

CHAPTER 2

RADIATION EFFECTS IN MICROELECTRONICS

2.1 Introduction

Electronic components deployed in a radiation-rich environment are constantly bombarded by a spectrum of energetic photons and particles. Reliable component operation mandates that the nuances of the radiation source, ambient temperature, and circuit bias conditions all be taken into account. Although protective shielding, error correction codes, and error scrubbing are all effective mitigation techniques for radiation-induced degradation, they inherently result in increased component cost and design complexity. An understanding of the underlying physical mechanisms behind component damage is therefore required to address the transient, permanent, and catastrophic failures of electronic components in a radiation-rich environments. The solutions to these problems will undoubtedly exercise numerous experimental and simulation tools at the material, device, circuit, and system levels.

Component degradation depends on the irradiation source, the particular energy loss mechanisms, the target material and its role in component function, and the physical principles upon which that function is based [16]. Regarding the target material, both metals and semiconductors are prone to defects caused by the energy-dependent removal of individual atoms from their lattice site following a nuclear collision with an energetic particle. The formation of these defects is known as *displacement damage* or *atomic displacement*. If the energetic particle is charged, then it also generates a line of electron-hole (e-h) pairs as it traverses through the semiconductor bulk. Failing recombination, any remaining (excess) electrons and holes may be coupled to a critical circuit node, resulting in any number of *single-event effects* (SEEs). Charged particles that traverse through dielectric materials also generate e-h pairs, which will either remain trapped in the dielectric or migrate to the semiconductor-dielectric interface; either outcome results in what is known as *ionization*

damage.

In this chapter an overview of the principal radiation effects in microelectronic devices and circuits is presented. An introduction to some of the fundamental parameters used in the measurement of radiation effects and a discussion of the physical mechanisms behind displacement damage, ionization, and SEEs in Si-based electronics are provided in Section 2.2. Space-based electronics and high-energy-physics experiments are cited as two examples of extreme environments in Section 2.3. In Section 2.4, a survey of the ground-based test facilities used for data collection is provided, and the chapter is concluded in Section 2.5 with a review of SiGe HBT operation and a description of the SiGe technology platforms under investigation.

2.2 Radiation-Induced Damage Mechanisms in Microelectronic Devices and Circuits

The key parameters used in the measurement of radiation sources and their associated degradation in semiconductors are outlined in Table 1.

Table 1: Important parameters for the measurement of radiation-induced degradation in microelectronic devices and circuits.

Parameter	Definition	Units	Typical Values
Dose	Energy absorbed per target weight	rad(SiO_2)	10^1 to 10^6
Dose Rate	Dose per unit time	rad(SiO_2)/s	10^{-3} to 10^3
Source Energy	Incident particle energy	eV	10^3 to 10^{12}
Particle Fluence	Total Particles per unit area	particles/cm^2	10^{10} to 10^{15}
Particle Flux	Fluence per unit time	particles/cm^2·s	10^9 to 10^{12}
LET	Ionizing energy loss	MeV·cm^2/mg	10^{-3} to 10^2
NIEL	Non-ionizing energy loss	keV·cm^2/g	10^{-3} to 10^2

The *dose* parameter is used to describe the radiation levels associated with ionization in dielectric materials and has units of "rads." The term "rad" is literally translated as the "*r*adiation *a*bsorbed *d*ose" and is used to describe the energy absorbed per unit weight of the target material. This material-specific designation is appended onto the unit by indicating rad(SiO_2) or rad(Si) to indicate energy loss in SiO_2 or Si, respectively. Conversion from rads to other energy-density units is facilitated by writing [17]

$$1\,[\text{rad}] = 100\left[\frac{\text{erg}}{\text{g}}\right] = 6.24\times10^{13}\left[\frac{\text{eV}}{\text{g}}\right] \tag{1}$$

or

$$100\,[\text{rad}] = 1\,[\text{Gy}] = 1\left[\frac{\text{Joule}}{\text{kg}}\right]. \tag{2}$$

The particle fluence, particle flux, non-ionizing energy loss (NIEL), and linear energy transfer (LET) are concepts used to describe the radiation environment associated with particles that cause atomic displacement and single-event effects. The particle LET also facilitates the conversion between the ionizing dose (D) and particle fluence (Φ) for charged particles by writing [18]

$$D\,[\text{rad}(\text{SiO}_2)] = LET\left[\frac{\text{MeV}\cdot\text{cm}^2}{\text{mg}}\right] \times \Phi\left[\text{cm}^{-2}\right] \times 1.6 \times 10^{-5}\left[\frac{\text{mg}\cdot\text{rad}\,(\text{SiO}_2)}{\text{MeV}}\right]. \tag{3}$$

2.2.1 Atomic Displacement in Silicon

Energetic particles incident on bulk Si may lose energy via a non-ionizing process such as atomic displacement. Among the earliest work on radiation effects in semiconductors was a series of studies on displacement damage in both Si and Ge substrates [19][20]. The results of these studies indicated that the resistivity of both n- and p-type Si samples increased as a result of atomic displacement following bombardment with alpha (α)-particles. Displacement damage occurs when an energetic particle undergoes a nuclear collision with an atom, thereby disrupting the lattice structure. The resultant aperiodicity in the bulk is synonymous with the creation of a vacancy (V) where the atom used to be and an interstitial (I) where the displaced atom now sits. This displaced atom is known as a *primary-knock-on atom* (PKA). Displacement damage may also be indirectly caused by x-rays and gamma (γ)-rays as a result of *Compton scattering* for photons between 70 keV and 20 MeV in Si [21]. Even though photons have insufficient momentum to displace an atom, the resultant high-energy Compton electrons can easily cause such displacement. As an example, it takes just 1 rad(SiO_2) of ^{60}Co gamma rays incident on Si to produce over 10^7 Compton electrons with energies up to 1 MeV [16].

Energy loss from the incident particle during atomic displacement is described using the NIEL concept to facilitate damage correlations in substrates irradiated with a variety of sources [22][23]. This approach is particularly useful for predicting system operation in a given radiation environment through the use of ground-based testing of a particular

mono-energetic particle. The particle NIEL is calculated over the solid angle integral of the differential cross section for atomic displacements as [24]

$$NIEL(E) = \frac{N_A}{A} \int_{\theta_{min}}^{\pi} \left(\frac{\partial \sigma (\theta, E)}{\partial \Omega} \right) T(\theta, E) \, L \left[T(\theta, E) \right] \partial \Omega, \tag{4}$$

where $T(\theta, E)$ is the average recoil energy, L is the Lindhard partition factor (which is used to delineate between ionizing and non-ionizing events), N_A is Avogadro's number (6.02×10^{23}), A is the atomic mass number, and θ_{min} is the scattering angle at which the recoil energy is equal to the displacement threshold. Alternatively, the particle NIEL may also be expressed analytically as [25]

$$NIEL = \left(\frac{N_A}{A} \right) \left[\sigma_e T_e + \sigma_i T_i \right], \tag{5}$$

where σ_e and σ_i are the elastic and inelastic capture cross sections, and T_e and T_i are the elastic and inelastic average recoil energies.

To create a PKA, the kinetic energy of the incident particle must be greater than the binding energy of the target atom to its nearest neighbors. The kinetic energy transferred during an atomic collision may be expressed as [16]

$$\triangle E_i = \frac{4A}{(1+A)^2} \sin^2 \left(\frac{\theta}{2} \right), \tag{6}$$

where E_i is the particle energy and θ is the angle through which the particle is deflected. The minimum $\triangle E_i$, known as the threshold energy (E_{th}), which is required for the creation of a vacancy-interstitial (V-I) pair in Si, is 21 eV. This value was determined using electron paramagnetic resonance (EPR) measurements on a Si-B1 center for phosphorus-doped n-type "100" Si irradiated with electrons with energies ranging from 0.7 MeV to 56 MeV [26]. V-I pairs in Si are known as Frenkel pairs and are typically short lived, with an annihilation rate of over 90% [25]. This high annihilation rate is a result of the fact that vacancies are highly mobile and readily annealed at temperatures well below 300 K [16]. Incident particles typically undergo a series of interactions with target atoms and create collision cascades, which instantaneously create many PKAs and vacancies along the particle track. The initial density of these PKAs and vacancies is proportional to the particle energy, and depending on the collision kinematics, those PKAs with sufficient energy and range go on

to produce collision cascades of their own – ultimately creating thousands more secondary (recoil) atoms and vacancies. As an example, a neutron or energetic light-ion will produce PKAs in Si with 50 keV of energy and a range (R_p) of 100 nm. Each 50 keV PKA can then generate additional recoils, which subsequently branch out from the charge track and ultimately produce a displacement tree spanning up to $0.1{\times}0.05$ μm^2 and generating over 2500 additional Frenkel pairs [27]. Each branch of this tree ends in a terminal cluster (near R_p) containing a high concentration of V-I pairs, where the NIEL values are typically highest [24]. It is in these terminal clusters that the most stable defect configurations form since the unrecombined vacancies and interstitials pair together to form higher-order configurations that are more stable. These higher-order defect configurations include di-vacancies (V-V), di-interstitials (I-I), multi-vacancies (V^n), multi-interstitials (I^n), and impurity complexes – such as phosphorus in n-type Si (V-P) or boron in p-type Si (V-B) [16]. In Si, the intrinsic vacancy defects (V^+ and V^+) and vacancy-impurity complexes ($(V\ Sn)^0$, $(V\ O)^-$, $(V\ P)^0$, $(V\ As)^0$, $(V\ Sb)^0$, $(V\ V)^+$, $(V\ Ge)^+$, $(V\ Ge)^-$, $(V\ Al)^+$, $(V\ B)^0$, $(V\ H_2)^0$, and $(V\ H)^0$) may assume a positive, negative, or neutral charge state. Conversely, trapped interstitial atoms (Al_i, B_i, C_i, and Si_iH_2) are typically neutral [28]. The dominant stable defects in Si are the $(V\ O)^-$ and $(V\ P)^0$ complexes, which are also known as A-centers and E-centers, respectively.

All of the defects described above result in disruptions to the Si lattice periodicity, which perturbs the local band structure [29]. Both the vacancies and interstitials can occupy energy levels at midgap ($E_T{\approx}\frac{E_G}{2}$) or near the band edges ($E_T{\approx}E_{C,V}$). The electrical activity of a given defect (or trap) is also a function of the trap concentration (N_T), the introduction rate (R_T), electron and hole capture cross sections ($\sigma_{n,p}$), irradiation temperature, measurement temperature, time after irradiation, thermal cycles following irradiation, injection level, material type, and impurity type and concentration [25][30]. Defect-induced levels in the bandgap can therefore be coupled to measurable device parametric shifts through carrier generation and recombination (G/R), carrier trapping, dopant compensation, tunneling, carrier scattering, and type conversion.

Midgap defect centers facilitate free-carrier generation through either a two-step process, in which a valence electron is thermally excited to E_T and then to E_C, or via hole emission from E_T followed by electron emission. This two-step process dominates at low level injection ($n_p \lll N_A$, $p_n \lll N_D$) when the free-carrier concentration is sufficiently less than at thermal equilibrium. Carrier recombination via these same midgap defect centers can be viewed as the reverse effect. In this case (recombination) an electron and hole may be separately captured at the E_T level where Shockley Read Hall (SRH) recombination reduces the G/R carrier lifetimes ($\tau_{g,r}$) [29]. This reduction in $\tau_{g,r}$ is the most important effect of displacement damage for BJTs, as it directly affects transistor gain, saturation voltage, storage time, and output sink current [31]. Alternatively, carriers may also be temporarily trapped at the shallow energy levels and later returned to the conduction or valence band without any recombination taking place (i.e., no reduction in $\tau_{g,r}$).

Deep-level transient spectroscopy (DLTS) measurements performed on p-type Si substrates that were irradiated with 1.5 MeV electrons have been used to isolate four carrier trap levels and the specific radiation-induced di-vacancy that controls lifetime [32]. Typically, shallow-level ($E_T \approx E_{C,V}$) traps dominate at high injection ($n_p \ggg N_A$,$p_n \ggg N_D$), whereas deep-level traps ($E_T \approx \frac{E_G}{2}$) dominate at low injection ($n_p \lll N_A$, $p_n \lll N_D$) [33]. Additional DLTS studies on both p- and n-type proton- and electron-irradiated Si samples have been used to identify the single negatively-charged acceptor state of the V-$V^{0/-}$ di-vacancy defect center (with a trap energy level of E_C-0.421 eV and capture cross section of 10^{-15} cm^2) as the dominant recombination center at low injection. At high injection levels, the A-center vacancy-oxygen impurity complex, V-$O^{0/-}$ (with a trap energy level of E_C-0.164 eV and a capture cross section of 10^{-14} cm^2), dominates the recombination process [34]-[36]. At low injection levels, the reduction in minority carrier lifetime can be expressed as [16]

$$\frac{1}{\tau} - \frac{1}{\tau_0} = K_\tau \Phi, \tag{7}$$

where K_τ is the minority-carrier-lifetime damage constant, τ and τ_0 are the post- and pre-irradiation carrier lifetimes, and Φ is the irradiation fluence. $K_\tau \Phi$ is dependent on the material type, incident particle type, operation temperature, injection level, and device

design. Damage factors are particularly useful because of the fact that over a known fluence range, the radiation-induced degradation can be assumed to be linear such that the impact on a particular parameter can be normalized to standard fluence values [37]. Damage factors can also be defined for many other parameters affected by radiation, including current gain and minority-carrier diffusion length.

Carrier removal and dopant compensation are the second most important impact of displacement damage since they result in increased resistivity (ρ) [38]-[43]. Both acceptor and donor atoms may be removed from their substitutional lattice sites, making them electrically inactive via the formation of a vacancy- or interstitial-impurity complex or through a dopant atom becoming a PKA and occupying an interstitial position [17]. Irradiation to extremely high fluence has even been used to create high-resistivity (MΩ·cm) substrates in Si for microwave circuits. This technique has been shown to be a viable alternative to traditional (and more costly) approaches such as SOI [44]. Radiation-induced deep traps may also change the Fermi level position (E_F), thereby reducing carrier density (n) and increasing ρ through the compensation of shallow dopants. The carrier removal rate for n- and p-type Si can be written as [45]

$$n\left(\Phi\right) - n\left(0\right) = K_n \Phi, \tag{8}$$

where $n(0)$ and $n(\Phi)$ are the pre- and post-irradiation carrier concentrations and Φ is the irradiation fluence. K_n is typically twice as large in p-type Si (compared to n-type Si) and is constant at low fluence, which means that the carrier density reduces linearly with fluence [45]. Type inversion may also occur when n-type bulk semiconductor material is converted to p-type via the introduction of acceptor ions from the displacement process [25]. This process has been shown to have detrimental effects for high-resistivity Si radiation detectors and p-type Si solar cells [41][42][44]. Defect levels may also enable trap-assisted tunneling through potential barriers or from the valence to conduction band and can be manifested as a tunneling component in the excess base current of SiGe HBTs [10]. Finally, atomic displacement is known to result in carrier mobility ($\mu_{n,p}$) reduction, which is caused by trapped carriers converting the defect centers into fixed-charge scattering centers [31][45].

Displacement damage is readily annealed over temperatures ranging from -200° C to 550° C. Individual vacancies and V-I complexes spontaneously dissociate at specific temperatures along this range under isochronal annealing using 15- to 30-minute time steps. Intrinsic vacancies dissociate at temperatures ranging from -200° C to -50° C, while the more stable di-vacancies and vacancy complexes dissociate at temperatures ranging from 150° C to 350° C [16]. Under isothermal annealing, the minimum temperature required for device recovery will depend on the dominant defect center. In the case of planar Si devices, temperatures well over 300° C are required because of the dominance of the V-O A-center [16], whereas for n-channel charge-coupled devices, damage dominated by the V-P E-center is readily annealed at 150° C [46].

2.2.2 Ionization in Silicon

Ionization damage in bulk Si originates from the creation of a "charged funnel track" along the path of the incident particles. Ionization in Si is studied using gamma- and x-ray photons, heavy ions, and sub-atomic charged particles such as protons and electrons. In this section the principal interaction mechanisms between ionizing radiation and bulk Si are reviewed following the discussion in [47].

2.2.2.1 The Interaction of Photons with Silicon

Photon interaction with matter is a strong function of both the photon energy (E_{ph}) and the atomic number of the target atoms (Z_T). The relative values of E_{ph} and Z_T determine whether the interaction is dominated by the photoelectric effect, Compton scattering, or pair production [21]. The photoelectric effect is the dominant mechanism for $E_{ph} \lll 0.5$ MeV. In this regime the entire quanta of photon energy may be absorbed by electrons in the innermost atomic shells (such as the K-shell). If E_{ph} is larger than the binding energy of the electron (B_e), then photon absorption results in the release of an electron from the atom with kinetic energy given by [47]

$$T = E_{ph} - B_e, \tag{9}$$

where the residual atom gains recoil energy in order to satisfy the conservation of momentum and energy. The ionization of the atom depends both on Z_T and the shell-dependent B_e, as described by [48]

$$(B_e)_K = Ry\,(Z-1)^2\,, \tag{10}$$

$$(B_e)_L = \frac{1}{4}Ry\,(Z-5)^2\,, \tag{11}$$

and

$$(B_e)_M = \frac{1}{9}Ry\,(Z-13)^2\,, \tag{12}$$

where $(B_e)_K$, $(B_e)_L$, and $(B_e)_M$ correspond to the K-, L-, and M-shell binding energies, respectively. Ry is the Rydberg constant, which can be written as [48]

$$Ry = hcR = hc\frac{2\pi^2 m_e e^4}{ch^3} = \frac{m_e e^4}{2\hbar^2} \equiv 13.61eV, \tag{13}$$

where R is the spectroscopic Rydberg constant for infinite mass (1.10×10^5 cm^{-1}), h is Planck's constant (6.63×10^{-34} m^2·kg/s), c is the speed of light (2.99×10^8 m/s), m_e is the electron rest mass (9.11×10^{31} kg), and e is the electronic charge(1.60×10^{-19} C). The total binding energy of the atom is typically expressed as $(B_e)_{tot} = 15.73 \times Z^{7/3}$ eV. At lower values of E_{ph}, photoelectrons are emitted in a direction that is perpendicular to the incident photons, but as E_{ph} is increased, the emitted photoelectron distribution peaks to a more forwardly-directed emission.

In Compton scattering, the incident photon impacts a nearly-free electron, causing it to recoil with a given kinetic energy given by [47]

$$T = E_{ph} - E_{ph}{}' = E - m_e c^2, \tag{14}$$

where E_{ph} is the incident photon energy, $E_{ph}^{'}$ is the scattered photon energy, and E is the total energy of the recoil electron. Conservation of momentum in the directions parallel (15) and perpendicular (16) to the incident photon generates [48]

$$\frac{hv}{c} = \frac{hv'}{c}\cos\theta_{ph} + p\cos\theta_e \tag{15}$$

and

$$0 = \frac{hv'}{c}\sin\theta_{ph} + p\sin\theta_e, \tag{16}$$

where $\frac{hv}{c}$ and $\frac{hv'}{c}$ represent the incident and scattered photon momentum, θ_{ph} and θ_e represent the scattering angle of the photon and Compton electron, and p is the momentum of the Compton electron. The difference between the wavelength of the incident photon (λ) and scattered photon (λ') is known as the Compton shift and is given by [48]

$$\Delta\lambda \equiv \lambda' - \lambda \equiv \frac{c}{v'} - \frac{c}{v} = \lambda_C(1 - \cos\theta_{ph}). \tag{17}$$

The maximum wavelength shift (corresponding to the maximum energy transfer) occurs for $\theta_{ph} = 180^o$ and is defined as $\Delta\lambda_{max} = 2\lambda_C$, where λ_C is the Compton wavelength. The scattered photon energy ($E_{ph(out)}$) can be expressed in terms of the scattering angle using [48]

$$\frac{E_{ph(out)}}{E_{ph(in)}} = \frac{hv'}{hv} = \frac{1}{1 + \varepsilon(1 - \cos\theta_{ph})}, \tag{18}$$

where a scattering angle of $\theta_{ph} = 180^o$ corresponds to the maximum $E_{ph(out)}$ and minimal Compton shift ($\Delta\lambda_{max} = 0$). The reduced incident photon energy is given as $\varepsilon \equiv hv/m_ec^2$. Additionally, the kinetic energy of the scattered photon T can be expressed as [48]

$$T = hv\frac{\varepsilon(1 - \cos\theta_{ph})}{1 + \varepsilon\,(1 - \cos\theta_{ph})} \tag{19}$$

or

$$T = hv\frac{2\varepsilon\cos^2\theta_e}{(1+\varepsilon)^2 - \varepsilon^2\cos^2\theta_e}. \tag{20}$$

Then, for $\theta_{ph} = 180^o$ and $\theta_e = 0^o$, the recoiled electron has its maximum kinetic energy T_{max} at [48]

$$T_{max} = \frac{hv}{1 + \frac{1}{2\varepsilon}}. \tag{21}$$

The scattering angles θ_{ph} and θ_e are related by the expression [48]

$$\cot\theta_e = (1+\varepsilon)\tan\frac{\theta_{ph}}{2}. \tag{22}$$

As the photon energy is increased further ($2m_ec^2 \ggg 1.02$ MeV), electron-positron pair production becomes the dominant mechanism. Excess energy over $2m_ec^2$ is converted to kinetic energy for both particles given by [47]

$$T_- + T_+ = E_{ph} - 2m_ec^2, \tag{23}$$

where E_{ph} is significantly larger than the sum of the kinetic energies (T_- and T_+). The excess energy here is accounted for in the rest mass of the electron and positron. The positron can be considered to be an "anti-electron," which upon slowing down will annihilate an electron, thereby releasing more gamma rays. These additional gamma rays will in turn interact with the material via either Compton scattering or the photoelectric effect [47].

2.2.2.2 The Interaction of Charged Particles with Silicon

The interaction of charged particles with matter is dominated by either Rutherford scattering or nuclear interactions. In 1911 Rutherford was able to derive the correct expressions for the differential cross section of a charged particle under the influence of a Coulombic force, leading to the discovery of the nucleus [49]. Rutherford's work was the result of analysis on experimental results from Geiger and Marsden [50][51], which showed surprisingly high levels of back-scattered α-particles being repelled from a gold foil target. These results contradicted the then widely accepted Thompson "plum pudding" model, which regarded the α-particle as a uniformly distributed cloud of positive charge.

In the new model, an incident particle with charge (Z_i) and mass (m_i) is assumed to approach a target atom of charge (Z_T) and mass (M_T). The coulombic interaction between the two particles results in a hyperbolic path of approach for the incident particle [48]. If the incident particle is presumed to have an initial velocity $\vec{u}$, then the principle of energy conservation yields the collision diameter b [48]:

$$b = \frac{Z_i Z_T}{\frac{1}{2} m_i u^2}. \tag{24}$$

The scattering angle is defined as: $\vartheta = \pi - 2\alpha$, and the corresponding differential cross section can be written as [48]

$$\sigma_R(\vartheta') \equiv \sigma_C(\vartheta) \equiv \frac{d\sigma'}{d\Omega'} \equiv \frac{b^2}{16 \sin^2\left(\frac{\vartheta'}{2}\right)} \equiv \left(\frac{Z_i Z_T}{\frac{1}{2}\mu u^2} \frac{1}{4 \sin^2\left(\frac{\vartheta'}{2}\right)} \right)^2, \tag{25}$$

where μ is the reduced mass given by [48]

$$\mu = \frac{m_i M_T}{m_i + M_T}. \tag{26}$$

The functional form relating the differential cross section σ_R to the scattering angle ϑ' is [48]

$$\frac{1}{\sin^4\left(\frac{\vartheta}{2}\right)}, \tag{27}$$

resulting in a maximized cross section for interaction for low scattering angles.

Although Rutherford scattering applies primarily to charged particles that undergo elastic scattering, several other mechanisms may dominate the ionization process. These include both the elastic and inelastic collisions with bound electrons and elastic and inelastic collisions with nuclei [48]. Particles with low energies (hundreds of eV) and low mass are more likely to undergo elastic collisions. Inelastic collisions with bound electrons are more probable for heavier particles such as mesons, protons, deuterons, and α-particles.

A quantum mechanical derivation developed by Hans Bethe in 1930 captures the rate of energy loss per unit path length, otherwise known as stopping power or LET, as a function of the properties of the incident heavy ion and target material as [52]

$$-\frac{dE}{dx} = \left(\frac{ze^2}{4\pi\varepsilon_0}\right)^2 \frac{4\pi Z\rho N_A}{Am_e v^2}\left[\ln\left(\frac{2m_e v^2}{I}\right) - \ln\left(1-\beta^2\right) - \beta^2\right], \tag{28}$$

where $v = \beta c$ is the heavy-ion velocity, ze is the heavy-ion electronic charge, x is the heavy-ion path length, A is the mass number of the target, Z is the atomic number of the target, I is the mean energy required to ionize an atom of the target, ρ is the density of the target material, N_A is Avogadro's number (6.02×10^{23}), and m_e is the rest mass of an electron. A simple conversion between "energy loss" and "charge deposition" for heavy ions is attained by writing

$$LET\left[\frac{\text{pC}}{\mu\text{m}}\right] = LET\left[\frac{\text{MeV}\cdot\text{cm}^2}{\text{mg}}\right] \times 2328\left[\frac{\text{mg}}{\text{cm}^3}\right] \times \frac{1.60\times10^{-19}\,[\text{C}]}{3.6\ [\text{eV}]}, \tag{29}$$

where it is assumed that Si has a density of 2328 mg/cm^3 and that an energy of 3.6 eV is required for the creation of one e-h pair [53]. This analysis yields a conversion factor of 0.01 when going from LET in units of MeV·cm^2/mg to units of pC/μm. The particle LET describes the energy loss to the target material via ionization processes and is analogous to the previously described NIEL concept, which is used to describe energy loss to the target material via non-ionization processes.

2.2.2.3 Single-Event Effects in Silicon

Ionization damage in the semiconductor lattice results in the creation of excess carriers in the bulk, many of which escape recombination. Failing recombination, these carriers are subject to the existing junction electric fields throughout the bulk and eventually migrate to the transistor terminals. This "collected charge" is then dissipated through the node with the lowest impedance and is coupled to the external circuit where it appears as any number of SEEs. *Single-event* (SE) is used to emphasize the fact that the effect stems from an *individual particle* interacting with the lattice. The earliest predictions of SE phenomena in microelectronics were made by Wallmark and Marcus in 1962 and were centered on the study of operational failures of highly integrated devices in a terrestrial environment. These failures were attributed to cosmic ray ionization and atomic displacement [54]. Observations of the first on-orbit satellite errors were attributed to galactic cosmic rays (GCR), as reported by Binder in 1975 [55]; however, it was not until 1979 that observations of terrestrial α-particle-induced single-event upset (SEU) phenomena in dynamic random access memories (DRAM) were observed by May and Woods [56].

The progression of SE phenomena from the initial ion strike to the device-, circuit-, or system-level response involves the distinct phases of charge deposition and charge collection. An energetic heavy ion interacting with bulk Si generates (either by direct ionization or nuclear interactions) a cascade of electrons, photons, and phonons. These reaction products have energies ranging from several electron-volts to a few mega electron-volts and are generated within 10 nm to 1000 nm of the ion track and between 10^{-13} s to 10^{-11} s after the ion strike [57]. Direct ionization (as described in Section 2.2) will occur as long as the particle has sufficient energy to release a sufficiently high density of e-h pairs. This is generally the case for heavy ions with an atomic mass number greater than two. Conversely, nuclear interactions typically involve an inelastic collision with a lattice atom, which generates both recoil daughter ions and reaction by-products. These interactions dominate for lighter particles such as electrons, protons, neutrons, and pions. As an example, a 30 MeV proton interacting with Si will deposit up to 10 MeV in a 2000 μm^3 volume via the three-step $^{28}\mathrm{Si}(\mathrm{P},\mathrm{P}\alpha)^{24}\mathrm{Mg}$ reaction, yielding 1 MeV phosphorous, 0.24

MeV Si, and 0.76 MeV Mg compound nuclei recoils, each with a projected range of between 0 μm to 5 μm [58]. A 7 MeV proton (with a range of 400 μm) and a 5.3 MeV α-particle (with a range of 27 μm) are also produced by this reaction [58]. These reaction products are much heavier than the original protons and can therefore deposit greater density of e-h pairs.

Between 10^{-12} s to 10^{-6} s after the ion strike, energy is transferred to conduction-band electrons and valence-band holes spatially located within 0.1 μm to 10 μm around the event, drastically increasing the localized excess e-h pair density [57]. These carriers are then subjected to drift-dominated transport caused by the junction electric fields, diffusion-dominated transport resulting from the carrier concentration gradients (generated by the ion strike), and heavy-ion-induced effects such as charge funneling and potential modulation [59]. Charge funneling refers to the process whereby the local electric fields collapse as a result of the conductive ion track interacting with the junction depletion region, effectively extending the electric fields deep into the substrate, which results in an increased charge collection volume [60]-[62]. The collection of unrecombined electrons occurs up to 10^{-6} s following the ion strike and spreads throughout hundred's of microns of metal wiring. This effectively increases the capacitance charge stored in the circuit and ultimately leads to the perturbation of nodal voltages and currents [57]. Depending on the details of the circuit application, this excess charge is manifested as one (or a combination) of many SEEs that may be classified as permanent, transient, destructive, or non-destructive.

Non-destructive SEEs are composed of transient events such as single-event upset (SEU), singe-event multiple bit upset (MBU), single-event transient (SET), single-event disturb (SED), and single-event functional interrupt (SEFI). SEU is simply the unintentional switching of a digital logic state following an ion strike. SEUs have been widely studied in both dynamic-(DRAM) and static-(SRAM) random access memories, microprocessors, and digital signal processors. In DRAM technologies, the designation of a stored bit is determined by the accumulation ("0") or depletion ("1") of electrons in the potential well under a polysilicon field plate. Following an ion strike, the well is flooded with electrons, which

reinforces a stored "0" but erases a stored "1" – resulting in a storage cell error [63]. Bit-line errors in DRAM also occur for ion strikes to the source and drain nodes of the access transistors [63][64] and may occur in concert with a storage cell error to produce a combined cell-bit SEU occurrence [65].

SEUs have also been widely studied in 4T SRAM cells. In these circuits, the reverse-biased body-to-drain *pn*-junction of an off-state transistor is the sensitive node [66][67]. After an ion strike, the transient current resulting from the "hit" transistor is compensated for by a current sourced from the other transistor in the affected inverter pair, which results in a voltage drop at its node and an incorrect memory state being written to the cell. The severity of this SEU is dependent upon whether the hit transistor is "off" or "on," the location of the ion strike relative to transistor potential wells, the feedback of the voltage transient through the cross-coupled inverter, and the time constant for the dissipation of the initial transient [68]-[70]. BJTs are also prone to SEU as a result of drift transport to the collector node via the electric field of the reverse-biased substrate-to-sub-collector (SxC) and base-to-collector (BC) junctions [71][72].

Memory and logic elements with closely spaced nodes are also vulnerable to MBUs. In the case of a DRAM cell, an MBU can occur when an ion strike in between any two potential wells shunts the generated charge from one node to another [73][74]. MBUs may also be observed for an ion strike at a grazing angle (greater than 60^{o} C) whose path traverses multiple nodes in high-density SRAM blocks [75]. SETs refer to the voltage transients at circuit nodes from an ion strike and are the underlying cause of several of the SEU phenomena described above. They are investigated both at the device and circuit level by measurement of their amplitude and duration and have been reported to affect digital and analog circuits, optocouplers [76][77], operational amplifiers [78]-[80], comparators [80]-[81], and analog-to-digital converters (ADCs) [82]-[85].

SEDs and SEFIs are used to describe the temporary corruption of digital information or a functional failure of control logic [57]. SEDs can occur when an error is read from an unstable SRAM cell within 10^{-3} s of an ion strike, even if the event does not cause a conventional SEU [86]. SEFIs occur at the system level in electrically-erasable programmable read-only

memory (EEPROM), DRAM, and DSPs, often rendering the component non-functional and requiring a system reset [87]-[89].

Destructive SEUs are permanent events such as single-event burnout (SEB), single-event latchup (SEL), and single-event gate rupture (SEGR). SEBs typically occur in devices with inherent parasitic BJTs. After an ion strike, the localized potentials are perturbed such that the parasitic BJT is turned on, thereby creating a positive-feedback conduction path that renders the device in a failure-inducing high current state [90]. SEBs are widely observed in BJTs and power MOSFETs [91]-[97]. Latchup is another well-known failure mechanism in advanced ICs and is triggered by the activation of a thyristor structure, such as the n(NMOS source)-p(substrate)-n(N-well)-p(PMOS drain) structure that can be found in most CMOS technology platforms. This failure mechanism usually occurs as a result of excessive voltage, incorrect power sequencing, and excessive substrate or N-well currents [98]. An SEL is simply a special case of latchup that is induced by excessive substrate and n-well currents following an ion strike. SELs have historically been observed in both CMOS [99]-[106] and complementary bipolar technologies. Finally, SEGR refers to the dielectric breakdown as a result of the high electric field associated with an ion strike and has been noted to occur in power MOSFETS [91][92]-[112] and highly scaled logic and memory ICs [113]-[116].

2.2.3 Ionization in Silicon Dioxide

Interest in the effects of ionizing radiation in microelectronic dielectrics increased in response to the failure of the communications satellite "Telstar 1" [117]. Surface degradation in the mesa-type bipolar devices of the onboard circuitry was identified as the primary failure mechanism and was attributed to electronic pumping of the Van Allen belts from several detonations of high-altitude nuclear devices [118]. The passivation utilized in gate and field oxides as well as inter-metal dielectric are the main areas of interest for ionizing radiation effects in SiO_2. Ionization in SiO_2 is a four-step process involving the generation of e-h pairs (*charge yield*), hopping transport of unrecombined holes through localized states in the SiO_2, deep-hole trapping at the Si/SiO_2 interface, and the creation of radiation-induced

interface traps within the bandgap [119].

2.2.3.1 Charge Yield

An energetic particle or photon interacting with bulk SiO_2 in the presence of an electric field generates e-h pairs at a cost, known as the pair creation energy (E_p), of 17 eV [120][121]. As a result of the differences in the electron and hole mobilities in SiO_2 at room temperature (20 $cm^2 \cdot V/s$ and 10^{-4} $cm^2 \cdot V/s$ respectively) [122], electrons are swept out of the oxide within 10^{-12} s [123]. Between 10^{-12} s to 10^{-6} s after the ionizing event, a percentage of the holes remains unrecombined and trapped in the bulk SiO_2 [119]. This fraction of unrecombined holes, known as the charge yield (N_h), can be written as [21]

$$N_h = f_y(E_{ox}) g_o D t_{ox}, \tag{30}$$

where $f_y(E_{ox})$ is a field-dependent expression for the hole fraction escaping initial recombination, g_o (8.1×10^{12} $cm^{-3} \cdot rad^{-1}$ (SiO_2)) is a material-dependent parameter that accounts for the oxide chemistry, D is the radiation dose, and t_{ox} is the oxide thickness. The $f_y(E_{ox})$ parameter in (30) is a function of the electric field in the oxide (E_{ox}) and the initial density of e-h pairs, which is in turn a function of the particle type, energy, and LET [124] [125].

The initial density of e-h pairs determines the appropriate regime for recombination, which is in turn determined by the relationship between the thermalization distance (r_t) and the mean separation distance (λ). r_t is the average separation between electrons and holes after thermalization and ranges from 5 nm to 10 nm in SiO_2; λ is inversely proportional to particle LET [119]. If $\lambda \ggg r_t$, then the *geminate* recombination model is invoked and recombination is only considered between individual members of the same e-h pair [126]. Weakly ionizing radiation, such as secondary high-energy electrons from ^{60}Co gamma rays, fall within this regime. As an example, 1 MeV electrons in SiO_2 yield an e-h pair density of 2×10^5 cm^{-1}, which is equivalent to a 50 nm pair separation distance [119]. Alternatively, for $\lambda \lll r_t$ the *columnar* recombination model is invoked, and the e-h pairs are assumed to have lost their individual identity with recombination processes considered to act on many electrons and holes occupying a cylindrical distribution around the particle track [125][127]. Columnar recombination is more appropriate for strongly ionizing particles such as low-

and medium-energy protons, α-particles, and heavy ions. As an example, 1 MeV protons in SiO_2 yield a line density of 3.33×10^7 cm^{-1}, which is equivalent to a 0.3 nm pair separation distance [119]. Other radiation sources fall in between these two extremes. Experimental results on a variety of MOS structures demonstrate a gradual transition in $f_y(E_{ox})$ from zero to one as the e-h pair density is increased (taking into account particle type, particle energy, oxide electric field and temperature) [125][127]-[129].

2.2.3.2 Hole Transport

Theories of hole transport in bulk SiO_2 have been based on measurements of the recovery in the flatband voltage (ΔV_{FB}) in MOS capacitors or threshold voltage (ΔV_T) in MOSFETs during the initial charge relaxation phase. These measurements indicate that hole transport processes occur between 10^{-4} s and 10^3 s after the ionizing event, and that the device response is a function of the ambient temperature, electric field, oxide processing history, and oxide thickness [121][130]-[133]. Hole transport in SiO_2 has been modeled using the *trap-hopping* model [134][135] and the *polaron-hopping* model invoking a *continuous time random walk (CTRW)* process [136]-[139]. In the trap-hopping model there is a continuous exchange of holes between trap sites in the SiO_2 bandgap and those in the Si valence band. The nature of these exchanges is governed by the trap energy level (E_T), capture cross section (c_p), and ambient temperature (T) such that at any given time one particular trap has the most holes captured and dominates the transit process. Shallow traps dominate between 10^{-7} s and 10^{-1} s after the ionizing event, while deep traps, with substantially longer dwell times, dominate after 10^1 s. The rate of change of the hole concentration at a given trap level can be written as [135]

$$\frac{dp_T}{dt} = c_p p N_0 \exp\left(-\frac{E_T}{\beta}\right) - p_T e_0 \exp\left(-\frac{E_i}{k_B T}\right), \tag{31}$$

where k_B is Boltzmann's constant (8.61×10^{-5} $eV{\cdot}K^{-1}$), T is the absolute temperature, N_0 is the trap concentration at the valence band edge, β determines the energy-dependent change in trap concentration, and e_0 is the emission factor. The factor $k_B{\cdot}T$ known as the thermal voltage (0.0259 eV). The rate of change of the overall trap concentration for n traps

can be written as [135]

$$\frac{dp}{dt} + \sum_{i=1}^{n} \frac{dp_i}{dt} = -k_1 pF, \tag{32}$$

where F is the electric field and k_1 is a parameter that accounts for carrier mobility and other factors.

Hole transport can also be modeled using phonon-assisted tunneling through randomly distributed localized shallow trap states with an average separation of 1 nm in bulk SiO_2 [119]. Positively charged holes in SiO_2 distort the lattice, thereby developing a self-trapping site that migrates through the SiO_2 along with the hole. This process is known as polaron-hopping and is subject to fluctuations in the average hopping distance, activation energy, and bond angles [21]. The tunneling probability (λ_i) can be written as [131]

$$\lambda_i \propto \left[\exp\left(-2\beta l_i\right) \exp\left(-\frac{\triangle}{k_B T}\right) \right], \tag{33}$$

where β is a fitting parameter, l_i is the average spatial trap separation, and Δ is the activation energy for phonon-assisted tunneling. As shown in (33), λ_i decreases exponentially with the average spatial trap separation (l_i). The associated distribution in hopping time ($\Psi_{(t)}$) is defined as [131]

$$\Psi_{(t)} \sim t^{-\left(1+N_D \frac{4\pi}{3} R_D^3\right)}, \tag{34}$$

where N_D is the density of trap states and R_D is the ionization radius.

CTRW processes have been employed in the modeling of charge relaxation in SiO_2 using both measurements of ΔV_{FB} [140]-[142] and of the tunneling current in wet and dry oxide films following x-ray irradiation [143]. These device-level response functions are characterized using the functional form $F(\alpha, t/t_s)$, where α is a disorder parameter (transparent to temperature, applied field, and oxide thickness) describing the general shape of the response. These parameters affect only the time scale of the response (defined for $T \geqslant 140\ K$) as [119]

$$t_s = t_s^0 \left(\frac{t_{ox}}{a}\right)^{\frac{1}{\alpha}} \exp\left[\frac{\triangle\left(E_{ox}\right)}{k_B T}\right], \tag{35}$$

where a is the hopping distance, $(\triangle\left(E_{ox}\right) = \triangle_0 - bE_{ox})$ is the activation energy, $\alpha = 0.25$, $a = 1$ nm, $\Delta_0 = 0.65$ eV, $t_s^0 = 10^{-22}$ s, and $b = 0.05$ eV/MV/cm for SiO_2.

2.2.3.3 Radiation-Induced Oxide Trapped Charge

The charges associated with the SiO_2 bulk have been characterized as either *fixed oxide* charge, *mobile ionic* charge, *interface trapped* charge, or *oxide trapped* charge [144]. Fixed oxide charge ($Q_f N_f$) is a positive charge resulting from structural defects in the SiO_2, is located less than 250 nm from the Si/SiO_2 interface, and does not interact with the Si substrate. Mobile ionic charge ($Q_{it} N_{it}$) exists as a result of ionic impurities in SiO_2, including Li^+, Na^+, K^+, and H^+. Interface trapped charge is composed of both positive and negative components and is derived from structural defects, metal impurities, or radiation-induced defects that readily interact with the Si substrate and can be repeatedly charged and discharged. Oxide trapped charge ($Q_{ot} N_{ot}$) may also be positive or negative and is the result of electrons or holes trapped in the SiO_2 bulk. Although the details of charge yield and hole transport have been studied almost exclusively on MOS structures, these processes are still applicable to the oxides used in BJTs. Once the charge yield has been established and the holes begin their transport process, the BJT response is markedly different than the MOS response as a result of the device structure, Si doping, and the location of the electrodes. In both MOSFETs and BJTs, the holes that transport to an electrode or to the substrate are typically removed, while the remainder are trapped in the SiO_2 bulk for a significant time period, especially near the Si/SiO_2 interface.

Electron spin resonance (ESR) and capacitance-voltage (CV) measurements on gamma-irradiated MOS structures prepared using both dry and wet oxides have been used to identify the E′-center as the dominant defect site responsible for hole trapping [145]-[147]. An E′-center is formed when a hole is captured by an oxygen vacancy site in SiO_2, which breaks the weak Si-Si bond and forms a pair of trivalent Si atoms (one neutral and the other positively charged) [148]-[151]. This conclusion is supported by the high correlation of the E′-center signal with the midgap CV shift (ΔV_{mg}) as a function of gamma dose up to 10 Mrad(SiO_2) and over an isochronal anneal sequence from 0^o C to 3000^o C. Additionally, a strong decrease has been measured in the E′-center signal as surface SiO_2 is removed during a 50 nm/s SiO_2 etch-back experiment. Measurement of $\Delta V_{mg} C_{ox}$ isolates the bulk SiO_2 traps since at midgap the P_b centers associated with trivalent Si centers at the Si/SiO_2

interface are inactive [152]-[155]. A third known defect in SiO_2 is the non-bridging oxygen center, which has not been associated with radiation-induced hole trapping [156]-[158]. Although the E′-center is the dominant defect site for radiation-induced hole trapping, high-field stress experiments [159] and electron paramagnetic resonance (EPR) measurements on MOS capacitors subjected to negative bias high-field electron injection [160] have yielded other dominant defect sites associated with an observed bulk SiO_2 trapped charge.

Although $Q_{ot}N_{ot}$ is fixed, meaning that it does not exchange charge with the semiconductor on a time scale that can be detected by device measurements [161], trapped holes near the oxide do undergo a gradual de-trapping process, which is partially responsible for the long-term annealing beyond 10^2 s after the ionizing event. This result has been explained using a combination of an electron tunneling model [162]-[163] and a thermal emission model [164]-[167]. Electrons tunneling into the oxide recombine with trapped holes at the positively charged trivalent Si atom near the Si/SiO_2 interface and establish a so-called "tunneling front" at a distance of $X_m(t)$ from the interface. This tunneling front advances into the SiO_2 bulk at a rate of 0.2 nm per decade in time. This model explains the widely observed logarithmic annealing response as a function of time, assuming that there is a uniform trap density in the oxide. $X_m(t)$ is expressed as [163]

$$X_m(t) = \frac{1}{2\beta} \ln\left(\frac{t}{t_o}\right), \tag{36}$$

where β is a tunneling parameter that is determined by the barrier presented to the electrons and t_o is a time scale parameter determined by the transition rate to the closest traps. Thermal emission of trapped holes in defect sites into the valence band of the oxide enables them to rapidly hop to the interface and into the Si substrate. Similar to the tunneling front, a "thermal emission front" is established at a distance of $\phi_m(t)$ from the Si/SiO_2 interface. $\phi_m(t)$ can be expressed as [167]

$$\phi_m(t) = \frac{k_B T}{q} \ln\left[AT^2 t\right], \tag{37}$$

where A is the capture cross section. Assuming a uniform distribution of trap energy levels, as $\phi_m(t)$ progresses through the SiO_2, the recovery characteristic exhibits a logarithmic dependence on time.

Negative-bias annealing experiments have been used to demonstrate the reversibility of electron-tunneling-induced trap annealing by monitoring N_{OT}, as determined by ΔV_{MG}. In these experiments ΔV_{MG} was cycled back and forth at 100° C simply by switching between positive and negative bias. The results of these experiments led to a revised model of the E′-center [168]-[170]. In the new model, electrons tunneling into the Si/SiO_2 interface with the neutral trivalent-Si rather than the positively charged one. This creates a dipole structure that may facilitate the reformation of the original weak Si-Si bond, thereby regenerating the original oxygen-vacancy prior to hole capture. Alternately, if the trivalent Si atoms are too far apart, then the dipole remains in a metastable state where it can exchange charge with the substrate via the continuous capture and release of electrons and holes from the substrate [168]-[170]. Annealing of the E′-center via electron tunneling may also enable the creation of a dipolar amphoteric neutral e-h trap, which may lead to a fixed negative charge component.

2.2.3.4 Radiation-Induced Interface Traps

Chemical reactions involving molecular H_2 or holes trapped in the SiO_2 are the principal mechanisms behind the formation of Si/SiO_2 interface traps [171]. One model prescribes a slow N_{IT} buildup through a two-stage process involving the release of a "hydrogen related species" such as protons (H^+) during hole transport, followed by a bias-dependent H^+ transport to the Si/SiO_2 interface [172]. At the interface, an electron is captured from the Si substrate, and the H^+ reacts with an interfacial Si-H bond to form molecular H_2 and a dangling Si orbital. This process has an overall time constant between 10 s and 10^4 s, is responsible for greater than 90 % of the total N_{IT} formation [119], and has been used to explain V_{th} shifts and increases in low-frequency noise in MOSFET structures [173]-[176]. An empirical model for the overall change in interface state density (ΔN_{IT}) for the two-stage model can be written as [172]

$$\triangle N_{SS}(t) = N_{SS}^{\infty}\left(E_{OX1}, D\right) f\left(\frac{t}{\tau\left(T_2, E_{OX2}\right)}\right), \tag{38}$$

where $N_{SS}^{\infty}(E_{OX1}, D)$ is the saturation value of interface states and $f(t/\tau\left(T, E_{OX2}\right))$ is a function used to describe the long-term buildup in terms of the second-stage temperature

(T_2) and the second-stage SiO_2 electric field (E_{OX2}). The saturation value of interface states is given as [172]

$$N_{SS}^{\infty}\left(E_{OX1}, D\right) = AD^{\frac{2}{3}} \exp\left[\beta\sqrt{E_{OX1}}\right], \tag{39}$$

where A and β are fitting parameters, D is the irradiation dose, and E_{OX1} is the first-stage SiO_2 electric field.

Fast charge pumping measurements on polysilicon gate MOSFETS have resulted in a ΔN_{IT} buildup that occurred too quickly to be explained by the two-stage model [177]-[180]. This inconsistency has led to N_{IT} formation being modeled as a prompt process in which holes are trapped near the Si/SiO_2 interface, convert to interface states with a time constant less than 10^{-3} s at room temperature, and account for less than 10% of N_{IT} formation [119]. Once the hole reaches the Si/SiO_2 interface, it breaks a Si-H bond and creates a dangling bond, which releases an H_2 molecule. Additionally, the reaction time constant balloons from 10^{-3} s at 300 K to $10^{\ 3}$ s at 200 K, which is consistent with a sharp decrease in hole transport at lower temperatures, indicating that hole transport could be the limiting step [179].

Electrical and ESR measurements on SiO_2 structures irradiated at cryogenic temperatures and subject to subsequent isochronal anneals have resulted in a marked increase in N_{IT} at 120 K and is coincident with the mobilization of a neutral molecular H_2 species [180]. Beyond 120 K, a plateau in N_{IT} is observed until 200 K at which point a further bias-dependent increase is observed, which is consistent with the previously described models relying on H^+ transport. The time constant for these reactions is around 10^{-3} s and accounts for about 10% of N_{IT} formation [119][181].

ESR measurements on "100" and "111" Si have identified the P_{b0} (on both "100" and "111") and P_{b1} (only on "111") variations of the previously described P_b-centers [152]-[155] as the defect sites common to the Si/SiO_2 interface. The P_{b0} center is a trivalent Si atom with three Si-Si bonds at the interface and a fourth dangling bond perpendicular to the interface for both the "100" and "111" orientation, whereas for the P_{b1} center the dangling fourth bond is at an angle to the interface [154][155][182]. Radiation-induced interface-state

formation is generally thought to be dominated by the P_{b0}-centers, as no increase in P_{b1}-centers has been observed with irradiation and the P_{b1} centers are thought to be electrically inactive [183] [184].

2.3 Extreme Environment Electronics

Microelectronic devices and circuits are routinely used in a variety of radiation-intense environments. Common examples include satellites to be deployed in the space environment [185][186], diagnostic equipment used for radiology in health care, control systems in nuclear reactors and weapons systems, detectors to be used in high-energy-physics experiments [187][188], consumer electronics operating in the natural environment [56][189], and semiconductor fabrication sequences such as ion implantation, plasma deposition, and reactive ion etch (RIE) [190]. The focus of this dissertation will be on the application of SiGe BiCMOS technologies for space-based electronic applications and high-energy-physics detectors.

2.3.1 Space-Based Electronic Components

Though appearing peaceful from earth, the solar system presents a very harsh environment for electronics. Space-based electronic systems are required to withstand temperature fluctuations from -180^{o} C to 120^{o} C on the surface of the moon and -230^{o} C in the shadowed polar craters [191]. Moreover, these systems are subject to a vast array of energetic particles that range in energy from a few kilo-electron-volts to several giga-electron-volts and are either trapped by the earth's magnetic field or transit through the earth's solar system [192][193]. The space-based environment may be broadly classified as trapped radiation, solar flares, or cosmic rays [16].

Trapped radiation consists primarily of the *Van Allen* radiation belts, which are composed of electrons, protons, and heavy ions trapped in the earth's magnetosphere [194]. The electron environment features particles with energies up to $7{\times}10^{6}$ eV split into two high-flux zones: a low-energy inner belt extending 2.4 earth radii (R_e) out from the mesosphere and an outer belt, with the highest energy electrons extending from 2.8 R_E to 12 R_E out from the mesosphere [16]. Trapped protons have energies up to $1{\times}10^{9}$ eV with a flux varying

inversely with energy out to about 3.8 R_E [195]. Solar flares are emitted by the sun in bursts, known as coronal mass ejections, during solar storms and are composed of energetic protons with energies up to 1×10^9 eV, α-particles, heavy ions, and x-rays.

Cosmic rays can be galactic, solar, or terrestrial. Galactic cosmic rays (GCR) originate from outside the solar system and are composed of low-flux, high-energy (from 1×10^6 eV to 1×10^{11} eV) particles passing through the solar system. The typical GCR composition is 85% protons, 14% α-particles, and 1% heavy ions [16]. Solar cosmic rays (SCR) are created from solar flares that eject a stream of protons, α-particles, and heavy ions similar to the GCR spectrum but with different relative contributions. Solar flares may last from several hours to a few days and are heavily modulated by the solar cycle. Finally, the cosmic radiation that penetrates the earth's atmosphere is transformed by several interactions to create cascades of secondary radiation being observed as cosmic radiation at the earth's surface.

The environment encountered by a satellite in orbit depends on many factors, including the trajectory, solar activity, and mission length. *IEEE Standard 1156.4* is used to classify these orbits as low- (LEO), medium- (MEO), geostationary- (GEO), and highly-elliptical- (HEO) earth orbits [18]. LEO paths take the satellite through the Van Allen belts several times during a 24-hour period with an altitude of between 200 km and 600 km. In the case of HEO, the altitude is in the range of 30,000 km, resulting in longer exposures to cosmic and solar flare environments [17]. Space environment models include the popular CREME 96 code, CHIME, and MACREE [196]-[198].

2.3.2 High-Energy-Physics Particle Detectors

Particle detectors deployed in high-energy-physics (HEP) experiments currently underway at the Large Hadron Collider (LHC) at the European Center for Nuclear Research (CERN) are exposed to particles with some of the highest energy and fluence of any electronic system. Among the goals of these experiments is the study of short lifetime subatomic particles such as bosons, muons, and quarks produced from 7 TeV protons colliding in a cyclotron with a radius of 4.3 km at a collision rate of 10^9 collisions/s [199]. In these

experiments, the low probability of nuclear reactions requires a large number of collisions, and therefore a large fluence, to observe the desired events.

Currently there are four experiments positioned around the LHC ring. A Toroidal LHC ApparatuS (ATLAS) and Compact Muon Solenoid (CMS) are designed to study proton-proton collisions, the Electromagnetic CALormimter (ECAL) measures electron and proton energies, the Hadronic CALormiter (HCAL) measures the energy of hadrons produced by the proton-proton collisions, and the Muon Detector measures the trajectory and energy of the muons [200]. These detectors are exposed to a radiation environment dominated by protons and neutrons with a negligible percentage of heavy ions. In this environment, ionization, displacement damage, and soft errors such as SEU, SET, or SEFI is the main degradation mechanisms, while heavy-ion-induced degradation such as SEL or SEGR are rarely observed. The highest ionizing radiation levels observed in the innermost tracker of ATLAS approaches 2.7×10^7 rad(SiO_2). In addition, detector electronics must be tolerant to 1 MeV neutron equivalent fluence values near 4.7×10^{14} n/cm^2) and proton fluence values near 5.4×10^{14} p/cm^2) [200].

2.3.3 Radiation Test Facilities

2.3.3.1 Protons

Proton irradiation was performed at three facilities with varying energy and flux capabilities. Low-energy protons were obtained from the Leach Science Center at Auburn University, medium-energy protons from the Crocker Nuclear Laboratory at the University of California at Davis, and high-energy protons from the European Center for Nuclear Research IRRAD-1 facility.

1. Leach Science Center (LSC) [201] – At LSC, protons with energies ranging from 1.75 MeV to 4.0 MeV are provided over a 2.5 cm diameter with 88% uniformity using a National Electrostatics Corporation (NEC) 2 MV 6SDH-Pelletron tandem accelerator. The accelerator is equipped with a RF charge exchange ion source in addition to a SNICS heavy-ion source and is capable of irradiation with dose rates ranging from 50 rad(SiO_2)/s to 1 krad(SiO_2)/s [202]. Samples are irradiated in a vacuum chamber to

minimize straggling.

2. Crocker Nuclear Laboratory (CNL) [203] – At CNL, protons with energies ranging from 1.25 MeV to 68.0 MeV and flux ranging from 10 p/cm^2·s to 10^{11} p/cm^2·s over a 2.75″ diameter with 90% uniformity are provided using a 76″ variable energy isochronous cyclotron [204]. Dosimetry measurements are made using a five-foil secondary emission monitor calibrated against a Faraday cup. Deuteron and α-particle beams with maximum energies of 45 MeV and 60 MeV are also available.

3. European Center for Nuclear Research (CERN) [205] – At CERN, protons with an energy of 24 GeV are obtained using the IRRAD-1 irradiation zone at the CERN PS east hall using beam PS-T7. The beam spot size is 2×2 cm^2 with flux ranging from 3×10^9 p/cm^2 · s to 9×10^9 p/cm^2 · s [206].

2.3.3.2 Gamma rays

Gamma irradiation was performed at the Radiation Effects Facility at the NASA Goddard Space Flight Center and at the Solid State Gamma Irradiation Facility at Brookhaven National Labs.

1. NASA Goddard Space Flight Center (NASA-GSFC) [207] – At NASA-GSFC gamma rays are provided using a J.L. Shepherd Model 81 ^{60}Co source, which is contained in a 20×20 ft^2 shielded room with a viewing window, high ceiling, and raised floor to minimize back-scattering. Dose rates vary from 1.67×10^{-4} rad(SiO_2)/s to 5.00×10^1 rad(SiO_2)/s and are dependent on the distance between the irradiation source and the sample.

2. Brookhaven National Laboratory (BNL) [208] – At BNL gamma rays are provided using a 1.2 MeV ^{60}Co source, which is encased in a stainless steel cylinder placed in a 14×14 ft^2 chamber surrounded by a concrete block designed to minimize back-scattered gamma rays. There is also a 1-mm aluminum shield to prevent the absorption of low-energy scattered electrons. Dose rates vary from 2.78×10^4 rad(SiO_2)/s

to 5.56×10^{1} rad(SiO_2)/s and are dependent on the distance between the irradiation source and the sample.

2.3.3.3 Neutrons

Neutron irradiation was performed in a 250 kW TRIGA Mark II light-water reactor with an annular graphite reflector cooled by natural convection using a Radium-Beryllium (Ra-Be) neutron source with a flux of 1.00×10^{6} n/s [209], at the Jozef Stefan Institute in Ljubljana [210]-[213]. Both fast neutrons (with an energy of 1×10^{5} eV) and thermal neutrons (with an energy of 0.0259 eV) are produced in a 1:2 flux ratio. A cadmium shield shield is used to minimize the production of secondary particles [214].

2.3.3.4 X-rays

X-ray irradiation was performed at the Vanderbilt University Radiation Effects Research Group [215] using an ARACOR test system that produces x-rays with energies ranging from 1×10^{4} eV to 6×10^{4} eV and dose rates ranging from 3.33×10^{-2} rad(SiO_2)/s to 3.33×10^{3} rad(SiO_2)/s [216].

2.3.3.5 Heavy-Ion Broadbeam

Heavy-ion broadbeam irradiation was performed at the K500 Superconducting Cyclotron Facility at the Texas A&M University Cyclotron Institute [217]. Ion beams with energies of 15 MeV/amu, 25 MeV/amu, and 40 MeV/amu enable testing with LET values ranging from 2.5 MeV·cm^2/mg to 93 MeV·cm^2/mg at normal incidence (0^o), extending up to 150 MeV·cm^2/mg at 75^o. The 15 MeV/amu beams include ^{20}Ne, ^{40}Ar, ^{63}Cu, ^{84}Kr, ^{109}Ag, ^{129}Xe, ^{141}Pr, ^{165}Ho, ^{181}Ta, and ^{197}Au; the 25 MeV/amu beams include ^{20}Ne, ^{40}Ar, ^{84}Kr, and ^{129}Xe; and the 40 MeV/amu beams include ^{20}Ne, ^{40}Ar, ^{84}Kr, and protons. Beams are delivered with a high degree of uniformity over a $1.8''\times1.8''$ area for samples irradiated in a vacuum and over a $1''$ diameter for samples irradiated in air.

2.3.3.6 Heavy-Ion Microbeam

Heavy-ion microbeam irradiation was performed at Sandia National Laboratory's Ion Beam Induced Charge Collection (IBICC) facility using a 6 MV High Voltage Engineering

EN Tandem van de Graaff accelerator equipped with a direct extraction source, an alphatros source, and two sputter sources [218]-[220]. Protons with energies up to 12 MeV are provided using the direct extraction source, ^{4}He ions with energies up to 18 MeV are provided using the alphatros source, and the sputter sources are used to provide practically any other heavy ion. Some of the most common ions include ^{12}C (up to 36 MeV), ^{16}O (up to 48 MeV), ^{28}Cu (up to 48 MeV), ^{35}Cl (at 35 MeV), ^{63}Cu (at 50 MeV), and ^{197}Au (up to 100 MeV). The microbeam is focused by imaging object slits with a minimum beam spot of 1×0.5 μm^2.

2.3.3.7 Pulsed Laser

Single-photon and two-photon pulsed laser irradiation was performed at the Naval Research Laboratory.

1. Single-Photon Absorption (NRL-SPA) [221][222] – Charge generation in the bulk semiconductor material following an ion strike can be emulated using a pulse of above-bandgap photons to generate e-h pairs [223]. At the NRL-SPA facility charge generation is accomplished using a cavity-dumped dye laser system capable of generating laser pulses 1.5 ps to 2 ps long with wavelengths ranging from 575 nm to 630 nm and 800 nm to 900 nm generated using the laser dyes *rhodamine 590* and *styryl 9*, respectively, at repetition rates between 1 kHz and 12 kHz [224]. Devices are irradiated on a motorized stage with 0.1 μm resolution and with optical pulses focused using a 100 X objective, yielding a Gaussian spot size of 1.2 μm at the air-to-material interface.

2. Two-Photon Absorption (NRL-TPA) [225] – At sufficiently high light intensity, two photons, each with energy below the bandgap, can be simultaneously absorbed to produce a single e-h pair. At the NRL-TPA facility, an amplified titanium sapphire laser system (Clark-MXR CPA1000) is used to produce optical pulses at 800 nm with a repetition rate of 1 kHz and a 120 fs pulse duration. A beta barium borate nonlinear crystal is used to tune the laser output to wavelengths ranging from 1.1 μm to 3.0 μm, which corresponds to photon energies ranging from 0.41 eV to 1.12 eV. Devices are imaged using a Si CCD and are irradiated on a motorized stage at 0.1 μm resolution.

The optical pulses are focused using a 100 X objective that yields a Gaussian spot size of 1.6 μm at the air-to-material interface.

2.4 SiGe BiCMOS Technology Platforms

Germanium (Ge) has long been identified as a suitable material for semiconductor device fabrication on account of its relatively high electron mobility $\mu_{n,Ge} \approx 3500$ cm$^2/V \cdot s^{-1}$ (at 300 K) [29]. From a manufacturing perspective, Si is far cheaper, easier to process, and much more abundant than Ge and is therefore at the core of the trillion dollar semiconductor industry. The idea of combining Si and Ge to leverage desirable electrical characteristics in a BJT was originally proposed in the 1950s [6]; however, it was not until the 1990s that advances in ultra-high vacuum/chemical vapor deposition (UHV/CVD) techniques enabled the realization of high-quality, epitaxial SiGe films at much lower thermal cycles than was previously possible. This advancement (UHV/CVD) has resulted in the fabrication of SiGe films with increased stability and improved dopant confinement [226]. Almost two decades following the realization of high-quality SiGe films, process maturation has resulted in several mature SiGe BiCMOS platforms currently in fabrication at over 40 commercial foundries [227]. SiGe BiCMOS is a technology that demonstrates performance levels comparable to materials in the exotic III-V world while leveraging an invaluable synergy with traditional low-cost, high-yield CMOS manufacturing.

2.4.1 Technology Development and Transistor Operation

In this section the fundamental principles behind the operation of SiGe HBTs are outlined following the discussion in [6]. A graded Ge profile across the boron-doped p-type base of a SiGe HBT creates a strained lattice structure in the base according to Vegard's rule [6]:

$$f_m(y) = \frac{a_{Si_{1-y}Ge_y}(y) - a_{Si}}{a_{Si}} = 0.042y, \tag{40}$$

where y is the Ge fraction, a_{Si} is the Si lattice constant, and $a_{Si_{1-y}Ge_y}$ is the lattice constant of the strained $Si_{1-y}Ge_y$ layer given as [6]

$$a_{Si_{1-y}Ge_y}(y) = a_{Si} + (a_{Ge} - a_{Si})y, \tag{41}$$

where a_{Ge} is the Ge lattice constant. This strain is translated into a Ge-induced offset in the bandgap at both the BE $\Delta E_{g,Ge}(x = 0)$ and BC $\Delta E_{g,Ge}(x = W_b)$ junctions of the SiGe HBT, as shown in Figure 1.

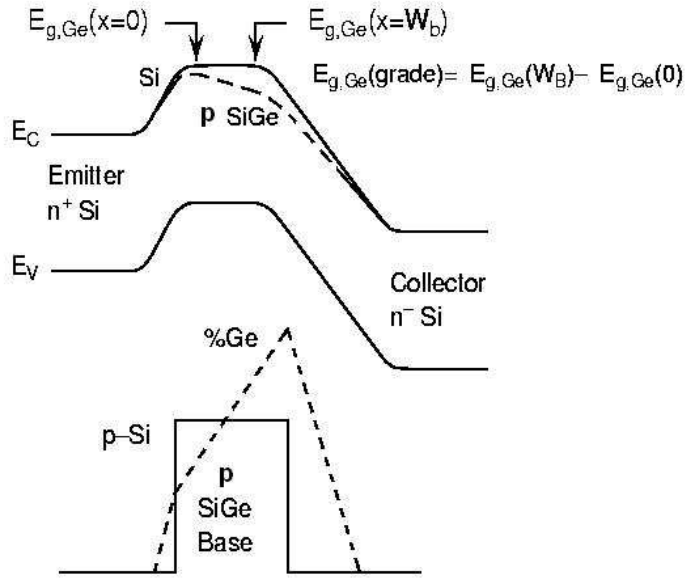

Figure 1: Germanium induced band offsets at the BE and BC junctions [6].

Since the Ge is graded across the width of the neutral base, the differences in band offsets translate into an additional Ge-induced drift field ($\Delta E_{g,Ge}(x = W_b) - \Delta E_{g,Ge}\,(x = 0)/W_b$), which results in an enhanced acceleration of the minority carriers in the base, thereby improving the frequency response of the device. Additionally, $\Delta E_{g,Ge}(x = 0)$ effectively translates into a lower barrier for electrons being injected from the emitter into the base so that for the same applied base-emitter voltage (V_{BE}), there is exponentially more electron injection. This increased electron injection translates into a larger collector current (I_C) and current gain (β) for the same base current (I_B) [228][229] and provides significantly more leverage in circuit design applications over conventional Si-based BJTs.

The expression for the collector current density ($J_C = I_C/A_E$) can obtained using the

Moll-Ross relations [230]:

$$J_C = \frac{q\left(e^{qV_{BE}/k_BT}-1\right)}{\int_0^{W_b} \frac{p_b(x)dx}{D_{nb}(x)n_{ib}^2(x)}}, \tag{42}$$

where x=0 and x=W_b correspond to the boundaries of the neutral base at the BE and BC junctions, $p_b(x)$ is the base doping profile, D_{nb} is the electron diffusivity in the base, V_{BE} is the base emitter voltage, and $n_{ib}(x)$ is the intrinsic carrier density in the base. $n_{ib}(x)$ can be written as [6]

$$n_{ib}^2(x) = (N_C N_V)_{SiGe}(x) e^{-E_{gb}(x)/k_BT}, \tag{43}$$

where $(N_C N_V)_{SiGe}(x)$ are the position-dependent Ge-induced offsets in the conduction and valence band edges and E_{gb} is the bandgap narrowing factor. E_{gb} can be written as [6]

$$E_{gb}(x) = E_{gbo} - \Delta E_{gb}^{app} + \left[\Delta E_{g,Ge}(0) - \Delta E_{g,Ge}(W_b)\right]\frac{x}{W_b} - \Delta E_{g,Ge}(0), \tag{44}$$

where E_{gbo} is the Si bandgap under low doping, E_{gb}^{app} is the apparent heavy doping bandgap narrowing in the base region, and $\Delta E_{g,Ge}(x)$ is the percentage Ge grading across the base, which can be written as [6]

$$\Delta E_{g,Ge}(grade) = \Delta E_{g,Ge}(W_b) - \Delta E_{g,Ge}(0), \tag{45}$$

The final expression for J_C in a SiGe HBT is then expressed as [6]

$$J_C = \frac{qD_{nb}}{N_{ab}^- W_b}\left(e^{qV_{BE}/k_BT}-1\right) n_{io}^2 e^{\Delta E_{gb}^{app}/k_BT}\left\{\frac{\tilde{\gamma}\tilde{\eta}\Delta E_{g,Ge}(grade)/k_BT e^{\Delta E_{g,Ge}(0)/k_BT}}{1-e^{-\Delta E_{g,Ge}(grade)/k_BT}}\right\}, \tag{46}$$

where $\tilde{\gamma}$ and $\tilde{\eta}$ represent the SiGe to Si ratio of the effective density of states and minority carrier diffusivity respectively. In (46) it can be seen that J_C is dominated by the $\Delta E_{g,Ge}(x=0)$ term in the exponent of the numerator. Moreover, in equally constructed Si BJTs and SiGe HBTs with comparable J_B, the enhancement in current gain (Ξ) at fixed V_{BE} can be written as [6]

$$\frac{\beta_{SiGe}}{\beta_{Si}}\Big|_{V_{BE}} = \Xi = \left[\frac{\tilde{\gamma}\tilde{\eta}\Delta E_{g,Ge}(grade)/k_BT\ e^{\Delta E_{g,Ge}(0)/k_BT}}{1-e^{-\Delta E_{g,Ge}(grade)/k_BT}}\right]. \tag{47}$$

As with J_C, Ξ exhibits an exponential dependence on $\Delta E_{g,Ge}$(x=0), but a linear dependence on $\Delta E_{g,Ge}(grade)$, which implies that a "box" profile is most suitable for β enhancement.

Additionally, since T is incorporated in the denominator of the exponent, these enhancements are even larger at cryogenic temperatures. The Ge profile can be tuned to match other parameters such as the Early voltage (V_A), the emitter and base transit times (τ_e and τ_b), and cutoff frequency (f_T). If V_A is written as [6]

$$V_A = J_C(0)\left\{\frac{\partial J_C}{\partial V_{CB}}\Big|_{V_{BE}}\right\}^{-1} \simeq J_C(0)\left\{\frac{\partial J_C}{\partial W_b}\Big|_{V_{BE}}\frac{\partial W_b}{\partial V_{CB}}\right\}^{-1}, \tag{48}$$

and the relevant substitutions made according to (42), then the Ge profile-dependent expression for the enhancement in V_A can be expressed as [6]

$$\frac{V_{A,SiGe}}{V_{A,Si}}\Big|_{V_{BE}} \simeq \frac{e^{\triangle E_{g,Ge}(grade)/k_BT}}{\triangle E_{g,Ge}(grade)/k_BT}. \tag{49}$$

The dynamics of carrier transport as it relates to the high-frequency operation of the transistor are dominated by the parameters τ_e, τ_b, and f_T. The Moll-Ross relationships for τ_b at low injection can be written as [6]

$$\tau_b = \int_0^{W_b} \frac{n_{ib}^2(x)}{p_b(x)}\left[\int_0^{W_b}\frac{p_b(y)dy}{D_{nb}(y)n_{ib}^2(y)}\right]dx, \tag{50}$$

and by utilizing the expression for n_{ib}^2 given in (43), the corresponding expression for τ_b in a SiGe HBT is [6]

$$\tau_{b,SiGe} = \frac{W_b^2}{\tilde{D}_{nb}}\frac{k_BT}{\Delta E_{g,Ge}(grade)}\left\{1 - \frac{\left(1-e^{-\Delta E_{g,Ge}(grade)/k_BT}\right)k_BT}{\Delta E_{g,Ge}(grade)}\right\}. \tag{51}$$

Furthermore, under the assumption of constant base doping and constant bandgap, (50) can be simplified for a Si BJT to yield [6]

$$\tau_{b,Si} = \frac{W_b^2}{2D_{nb}}. \tag{52}$$

The resultant Ge-induced τ_b enhancement is equivalent to (51), with the exception that $\frac{W_b^2}{\tilde{D}_{nb}}$ is replaced by a factor $\frac{2}{\tilde{\eta}}$. The emitter transit time enhancement is determined in a similar fashion and can be written as [6]

$$\frac{\tau_{e,SiGe}}{\tau_{e,Si}} \simeq \frac{J_{C,Si}}{J_{C,SiGe}} = \frac{1-e^{-\Delta E_{g,Ge}(grade)/k_BT}}{\tilde{\gamma}\tilde{\eta}\frac{\Delta E_{g,Ge}(grade)}{k_BT}e^{\Delta E_{g,Ge}(0)/k_BT}}. \tag{53}$$

The overall implications of the expressions (42)-(53) are that the Ge profile in the base can be tailored to optimize for different SiGe HBT performance figures of merit. Box profiles

with large $\Delta E_{g,Ge}(x = 0)$ are suitable for β enhancement, whereas a strong $\Delta E_{g,Ge}(grade)$ or large $\Delta E_{g,Ge}(x = W_b)$ yield improved V_A, τ_e, τ_b, and hence f_T. The advanced SiGe HBT profiles, such as the ones under investigation in this work, employ trapezoidal profiles in an attempt to achieve simultaneously good β, $J_{C,SiGe}$, V_A, and f_T.

2.4.2 IBM SiGe Technology Platforms

The teams at IBM Microelectronics were the first to fabricate SiGe HBT devices and as such their work allows for a comprehensive look at the trends in the scaling of the technology over four distinct generations [226]. Until recently, increased CMOS switching speed has been attained by continued reduction in minimum feature size, in keeping with Moore's Law. On BiCMOS platforms, the corresponding enhancement in BJT performance is attained primarily through vertical profile scaling and more aggressive dopant profiles.

The key performance metrics for the 1st- through 4th-generation SiGe HBTs under investigation in this work are illustrated in Table 2.

Table 2: 1st-, 2nd-, 3rd-, and 4th-generation HBT performance figures of merit.

Figure of Merit	1st(5HP)[231]	2nd(7HP)[232]	3rd(8HP)[233]	4th(9T) [234]
Actual W_E (μm)	0.42	0.18	0.12	0.12
peak f_T (GHz)	50	120	207	300
peak f_{max} (GHz)	70	100	285	170
BV_{CEO} (V)	3.3	2.5	1.7	1.4

The bulk SiGe HBTs investigated in this work are the IBM 1st- through 4th- generation technologies. The 1st generation SiGe HBT achieves a peak f_T of 50 GHz and is manufactured in a 0.5 μm CMOS compatible technology with a collector-emitter breakdown voltage (BV_{CEO}) of 3.3 V [231]. The emitter width (W_E) in 5AM is also 0.5 μm. The device is built on an $n+$ sub-collector (5-10 Ω/sq) on top of a $p-$ substrate (10-15 Ω-cm) with a lightly doped epitaxial $n-$ type collector. Polysilicon deep trenches (DT) are used to isolate adjacent devices, and shallow trench isolation (STI) oxides are used for internal isolation. The base is formed through the growth of a composite SiGe epitaxial layer, which is composed of a 10 to 20 nm Si buffer, a 70 to 100 nm boron-doped active layer, and a 10 to 30 nm Si cap in a trapezoidal Ge graded profile. A selectively implanted collector (SIC), which is

phosphorous-doped to 1x10^{17}/cm^3, is used to reach the sub-collector and reduce collector resistance (R_C). The emitter is arsenic-doped to 1x10^{21}/cm^3 and is fully self-aligned to the base using a BE spacer oxide. A polysilicon extrinsic base and silicided intrinsic base (5-10Ω/sq) facilitate transistor contact to the back-end-of-the-line (BEOL) metalization. In the 2$^{\text{nd}}$-generation device (IBM 7HP), lateral and vertical scaling methodologies are used to realize a W_E of 0.2 μm [232].

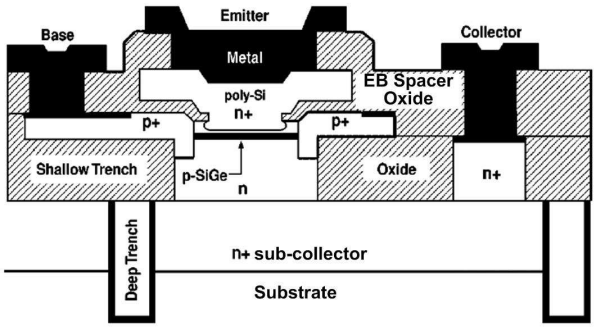

Figure 2: Cross section of 1$^{\text{st}}$- and 2$^{\text{nd}}$-generation HBTs [231].

A cross section of IBM 5AM and 7HP is illustrated in Figure 2, and the novel structure for the IBM 8HP and IBM 9T is illustrated in the cross section in Figure 3.

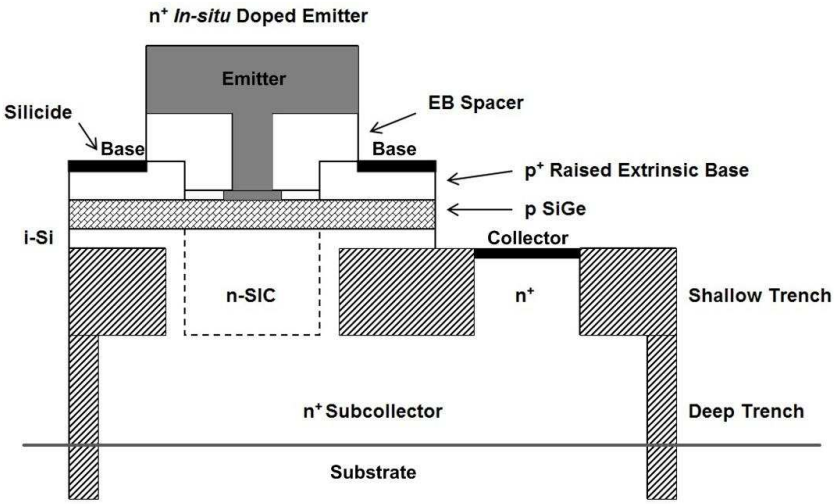

Figure 3: Cross section of 3$^{\text{rd}}$- and 4$^{\text{th}}$-generation HBTs [233].

In the 3$^{\text{rd}}$-generation SiGe HBT (IBM 8HP), an improvement in peak f_T (to 200 GHz) is

realized through fundamental changes in the physical structure of the transistor by the implementation of a "raised extrinsic base" structure, which reduces the collector-base overlay capacitance C_{CB} and features reduced thermal cycle processing [233] with a W_E of 0.12μm. The SiGe base region features an unconditionally stable 25% peak Ge profile deposited using UHV/CVD epitaxial growth techniques and doped with carbon, as described in [233]. The most advanced 4$^{\text{th}}$-generation technology shares the same representative cross section as the 3$^{\text{rd}}$-generation technology, with further performance enhancements realized through careful profile optimization and aggressive vertical scaling of the base and collector regions. These modifications yielded a then-record emitter-to-collector transit time (τ_{EC}) of 0.45 ps [234] and a corresponding peak f_T of 350 GHz. This frequency response represented a 67% increase over the previous performance record and was fabricated in a 120 nm Si compatible technology. The associated collector-to-emitter (BV_{CEO}) and collector-to-base (BV_{CBO}) breakdown voltages are 1.4 and 5.0 V, yielding an $f_T \times BV_{CEO}$ product well above the 200 GHz V "Johnson limit" [235]. Process windows currently enable the realization of peak f_T and f_{max} both above 300 GHz, as recently reported in [236] and [237]. The SiGe BiCMOS technologies presented here are commercially-available from IBM, and support a wide range of applications, from 2.4 GHz GSM and CDMA RF cellular, to 10 GHz X-band radar, to 60 GHz ISM communication systems.

CHAPTER 3

MEDIUM-ENERGY PROTON-INDUCED DEGRADATION

3.1 Introduction

In this chapter, the impact of 63 MeV proton irradiation on the performance characteristics of 1st- through 4th-generation SiGe HBTs is examined. First, the low-injection excess base current is introduced as the classical signature of radiation-induced degradation in SiGe HBTs. Second, 3rd-generation HBTs are used to illustrate the effects of medium-energy proton irradiation on several transistor parameters including the forward- and inverse-mode Gummel characteristics, forward-mode current gain, common-emitter output characteristics, avalanche multiplication, neutral base recombination, and low-frequency noise. In DESSIS, 2-D TCAD simulations of the carrier recombination rate are used to emulate the post-irradiation forward- and inverse-mode Gummel characteristics. Third, the influence of both transistor bias and mixed-mode electrical stress on the proton-induced degradation in 3rd-generation HBTs are presented. Fourth, the reversal of this proton-induced degradation in 3rd-generation HBTs is demonstrated using both isothermal and isochronal annealing. Finally, the implications of vertical and lateral technology scaling on the observed proton-induced degradation are investigated using comparisons of several *ac* and *dc* figures of merit.

The findings presented in this chapter indicate that SiGe HBTs exhibit impressive tolerance to medium-energy proton irradiation, even at unprecedented levels of technology scaling, and suggest that electronic components that are designed using SiGe BiCMOS technology should be considered for space-based electronic components.

3.2 Experiment Details

Proton irradiation at 63 MeV was performed at the CNL facility [203][204]. Except where stated, sample preparation, proton irradiation, and parameter measurement followed the same basic procedure, which is now described. Individual transistors, configured as *dc* test structures, were diced out of product wafers and packaged into 28-pin ceramic dual-in-line packages (DIPs). Once diced, each sample was attached to the ceramic substrate of the DIP using a two-part conductive silver epoxy, and the package was subsequently cured on a hot plate at 180^{o} C for 30 minutes. The terminal pads of two to three transistors for each sample were then wire bonded to the package leads using 1-mil gold wire. Pre-irradiation transistor characteristics were measured using an Agilent 4155 Semiconductor Parameter Analyzer (SPA). The DIPs were then mounted into custom-designed printed circuit boards (PCBs), which enabled irradiation to be performed with a bias applied to the transistor terminals. Post-irradiation transistor characteristics were measured after each incremental fluence using a custom-made test fixture and the Agilent 4155 SPA. After each post-irradiation measurement, the DIPs were then inserted into the beam for irradiation over another incremental fluence and then the transistor characteristics were measured again. The process of incremental irradiation and measurement steps is known as "in-situ" irradiation.

The packaging outlined above does not facilitate the measurement of broadband S-parameters, which are required to obtain f_T and f_{max}. To facilitate these measurements, another set of transistors, this time configured as *ac* test structures, were also diced out of product wafers. These *ac* test structures were not packaged, and were therefore irradiated without any bias applied to the transistor. The procedure of taking a single irradiation step followed by a single measurement step is known as "passive" irradiation. In passive irradiation, there is only one irradiation step, which is followed by one post-irradiation measurement step. In this case, pre- and post-irradiation measurements were made using an Agilent 8510C Vector Network Analyzer (VNA), and f_T and f_{max} were derived using the de-embedding techniques discussed in [238].

3.3 Radiation-Induced Excess Base Current

The physical mechanisms underlying the observed radiation-induced excess base current (ΔI_B) in BJTs are now presented following the discussion in [161]. For npn BJTs, the forward-mode I_B is a hole current that can be decomposed into four components representing carrier recombination in the BE depletion region (I_{B1}), the injection of holes from the base into the emitter (I_{B2}), recombination in the neutral base (I_{B3}), and impact ionization in the BC junction (I_{B4}). In a pristine device, I_{B2} is the dominant component of I_B, but after exposure to ionizing radiation, I_{B1} increases as a result of the interaction of radiation-induced Si/SiO_2 interface traps with the depletion regions of the BE and BC junctions, as outlined in Section 2.2.

If the BE junction is forward biased, which occurs for $V_{BE} \geqslant 0$ V, and the BC junction is reverse biased, which occurs for $V_{BC} \leqslant 0$ V, then the BJT is said to be operating in the "forward mode." In the forward mode, the increase in I_{B1} results from the interaction of the BE depletion region with Si/SiO_2 interface traps associated with the BE spacer. Conversely, in the inverse mode, the relevant interaction is between the BC depletion region and the Si/SiO_2 interface traps associated with the STI [239]. If atomic displacement is the dominant mechanism, then I_{B3} increases as a result of traps created in the bulk p-type base region.

At low injection, SRH recombination drives the increase in I_{B1}. The SRH recombination rate in the bulk (R_b) is defined as [240][241]

$$R_b = \frac{pn - n_i^2}{\tau_{n0}(p + p_1) + \tau_{p0}(n + n_1)}, \tag{54}$$

where τ_{n0} is the electron lifetime, τ_{p0} is the hole lifetime, and N_T is the bulk trap density. τ_{n0} and τ_{p0} are inversely proportional to N_T, and n_1 and p_1 are representative of the trap energy and can be written as [161]

$$n_1 = n_i \exp\left(\frac{E_t - E_i}{k_B T}\right) \tag{55}$$

and

$$p_1 = n_i \exp\left(\frac{E_i - E_t}{k_B T}\right), \tag{56}$$

where E_t is the energy level of the dominant radiation-induced trap. If radiation-induced traps exist at various energy levels, then (54) can be integrated over the entire bandgap to obtain the overall recombination rate. In Si, midgap traps dominate the overall SRH recombination rate since they capture electrons and holes with equal probability. This result is easily verified by setting the derivative of the denominator of (54) equal to zero and solving for n_1 to give [161]

$$n_1 = n_i \sqrt{\frac{\tau_{n0}}{\tau_{p0}}}, \tag{57}$$

which, if τ_{n0}=τ_{p0}, reduces to the midgap condition of n_1=p_1. In the event that τ_{p0}≠τ_{n0}, midgap traps still determine the recombination rate since the exponential dependence of n_1 on E_t is stronger than the square root dependence of n_1 on $\frac{\tau_{n0}}{\tau_{p0}}$. Therefore, the maximum value of R_b in (54) occurs for equal carrier concentrations (n=p), which necessarily occurs within the depletion region of any pn junction. Both atomic displacement and ionization can change both the location and the peak of R_b in (54).

At the Si/SiO_2 interface, which is also referred to as the surface, the SRH recombination rate can be written as [161]

$$R_s = \frac{p_s n_s - n_i^2}{\frac{1}{c_{ns} N_{Ts}} (p_s + p_{1s}) + \frac{1}{c_{ns} N_{Ts}} (n_s + n_{1s})}, \tag{58}$$

where c_{ns} is the electron capture coefficient, c_{ps} is the hole capture coefficient, and N_{Ts} is the areal interface trap density. All other terms in (58) are the same as defined in (54), with the exception that the subscript "s" indicates that they are evaluated at the Si/SiO_2 interface. R_s can also be written as [161]

$$R_s = s_p \triangle p_s = \sigma_p N_{Ts} v_{th} \tag{59}$$

or

$$R_s = s_n \triangle n_s = \sigma_n N_{Ts} v_{th}, \tag{60}$$

where σ_p is the capture cross section for holes, σ_n is the capture cross section for electrons, v_{th} is the thermal velocity (10^2 cm/s), s_p is the surface recombination velocity of holes, and s_n is the surface recombination velocity of electrons. The location of N_{Ts} in (58)-(60) translates into an increase in R_s after irradiation.

Prior to irradiation, the collector and base current densities for npn BJTs are written as [161]

$$J_C = \frac{qD_{nB}n_{iB}^2}{N_{AB}W_B}\exp\left(\frac{qV_{BE}}{k_BT}\right) \tag{61}$$

and

$$J_B = \frac{qD_{pE}n_{iE}^2}{N_{DE}L_{pE}}\exp\left(\frac{qV_{BE}}{k_BT}\right), \tag{62}$$

where D_{nB} is the diffusivity of electrons in the base, D_{pE} is the diffusivity of holes in the emitter, n_{iB} is the intrinsic carrier concentration in the base, n_{iE} is the intrinsic carrier concentration in emitter, N_{AB} is the acceptor doping in the base, N_{DE} is the donor doping in the emitter, W_B is the width of the neutral base, and L_{pE} is the diffusion length of holes in the emitter. After irradiation, the component of J_B that is dominated by recombination in the BE depletion region (J_{B1}) can be written as [161][242]

$$J_{B1} \propto \sigma_n N_{Ts} v_{th}, \tag{63}$$

at the Si/SiO_2 interface, and

$$J_{B1} \propto \frac{1}{\tau}\exp\left(\frac{qV}{2k_BT}\right), \tag{64}$$

in the bulk. If there is significant recombination in the base, then J_{B3} can be written as [161]

$$J_{B3} = \frac{Q_B}{\tau_B} = \frac{qW_Bn_{B0}\exp\left(\frac{qV_{BE}}{kT}\right)}{2\tau_B}, \tag{65}$$

where Q_B is the minority carrier charge stored in the base and τ_B is the minority carrier lifetime in the base.

3.4 Proton-Induced Degradation in 3rd-generation SiGe HBTs

3.4.1 Gummel and Current Gain Characteristics

The forward-mode collector (I_C=J_C×A_E) and base (I_B=J_B×A_E) currents of a 3rd-generation HBT, with an emitter area (A_E) of 0.12×4.0 μm^2, are plotted as a function of V_{BE} in Figure 4. This transistor was irradiated at room temperature with all terminals grounded (V_{SX}=V_C=V_B=V_E=0 V) to a cumulative fluence of 4×10^{13} p/cm^2. The equivalent dose for protons, which is plotted on the x-axis, can be calculated by substituting

8.57×10^{-3} MeV·cm^2/mg for the LET of a 63 MeV proton in (3). Using this calculation, proton fluence values ranging from 7.45×10^{11} p/cm^2 to 4.45×10^{13} p/cm^2 correspond to equivalent dose values ranging from 100 krad(SiO_2) to 6 Mrad(SiO_2). The family of curves in Figure 4 is referred to as the forward-mode Gummel.

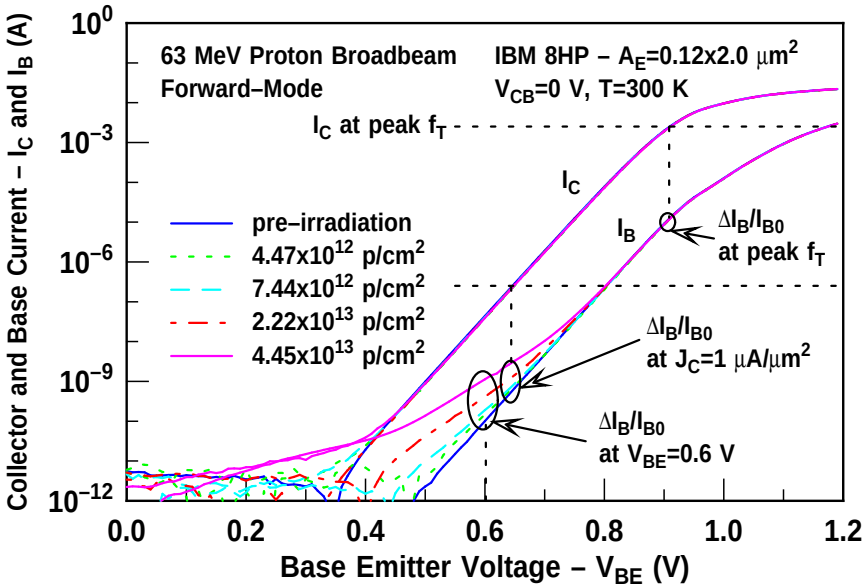

Figure 4: Forward-mode Gummel characteristics of 3rd-generation HBTs irradiated with 63 MeV protons to a cumulative fluence of 4.45×10^{13} p/cm^2.

As the proton fluence (Φ_P) is increased, there is a significant increase in I_B at low injection. From a measurement perspective, low injection is defined over V_{BE} values ranging from 0.4 V to 0.8 V. This low-injection ΔI_B is the classical signature of radiation-induced degradation in SiGe HBTs. To be sure, comparisons of the radiation-induced degradation as a function of transistor geometry, irradiation sources, and particle energies are facilitated using either the excess base current density (ΔJ_B) or the "normalized" excess base current $\left(\frac{\Delta I_B}{I_{B0}}\right)$, which can be expressed as

$$\frac{\triangle I_B}{I_{B0}} = \frac{I_{B\Phi} - I_{B0}}{I_{B0}}, \tag{66}$$

where $I_{B\Phi}$ is the post-irradiation base current and I_{B0} is the pre-irradiation base current. As shown in Figure 4, $\frac{\Delta I_B}{I_{B0}}$ may be evaluated at a specific base-emitter voltage, such as V_{BE}=0.6 V, or at a specific collector current density, such as J_C=1 μA/μm^2. Although

there is a significant increase in $I_{B\Phi}$ at V_{BE}=0.6 V, it should be noted that at circuit-relevant bias conditions, which are indicated by the trend line labeled I_C at peak f_T, there is no increase in $I_{B\Phi}$.

The forward-mode current gain (β), which is derived from the Gummel plot of Figure 4, is illustrated as a function of I_C in Figure 5. Coincident with the low-injection ΔI_B, there is a monotonic decrease in the maximum value of β (β_{peak}) along with a shift in the occurrence of β_{peak} to higher I_C. Although there is a 33% reduction in β_{peak} at 4.45×10^{13} p/cm^2, there is no change in β at peak f_T. In fact, the post-irradiation β at peak f_T is still greater than 200, which is more than sufficient for many RF, analog, and microwave circuits that use SiGe HBTs.

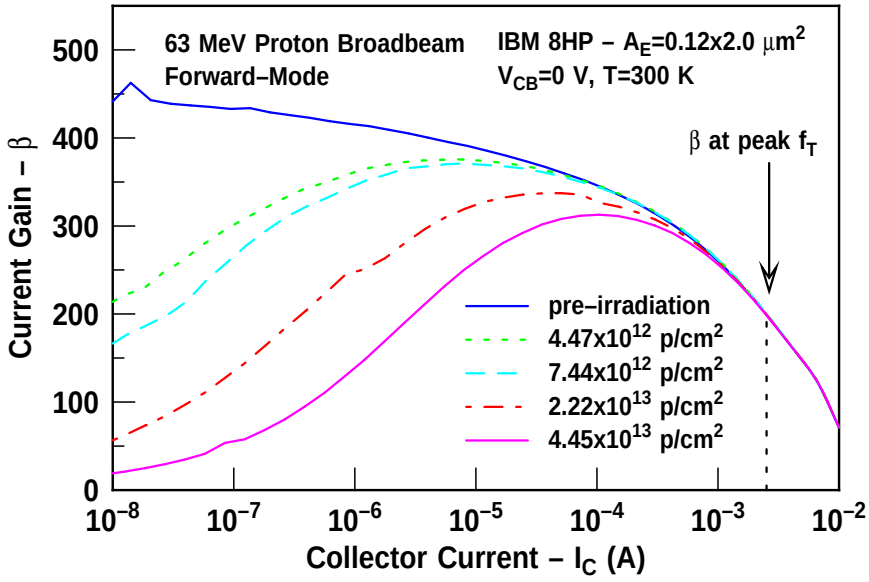

Figure 5: Forward-mode β of 3rd-generation HBTs irradiated with 63 MeV protons to a cumulative fluence of 4.45×10^{13} p/cm^2.

If the BE junction is reverse biased, which occurs for $V_{BE}\leqslant0$ V, and the BC junction is forward biased, which occurs for $V_{BC}\geqslant0$ V, then the transistor is said to be operating in the "inverse mode." During measurement, operation in the inverse mode is achieved by physically swapping the emitter and collector terminals so that the physical collector is now the electrical emitter and vice versa. The doping profiles typically used in SiGe HBTs are constructed to facilitate optimal operation in the forward mode, and most circuit applications

exercise the transistor in that configuration. One notable exception is the Merged Transistor Logic (MTL) architecture of the 1970s, which utilized operation in the inverse mode of the then state of the art BJTs to achieve low-power digital logic [243]. Unfortunately, there were several challenges involving the use of those transistors including large capacitances, low β, and low f_T, which when combined made MTL a far inferior technology platform to CMOS. Since then, the advancements in HBT technology scaling, which were outlined in Section 2.4, have yielded unintentional increases in the inverse mode performance of SiGe HBTs [244]. Moreover, the heavy-ion-induced charge collection on the emitter terminal is typically much smaller than on any other terminal, which suggests that inverse mode operation may be a viable SEE mitigation technique for HBT digital logic [14][245]. It is within this context that the TID response of SiGe HBTs operating in the inverse mode is addressed. In Figure 6, the inverse-mode Gummel is plotted for 3$^{\text{rd}}$-generation HBTs irradiated with 63 MeV protons to a cumulative fluence of 4.45×10^{13} p/cm^2. As was observed in the forward mode, the inverse-mode I_B increases as a function of Φ at low injection.

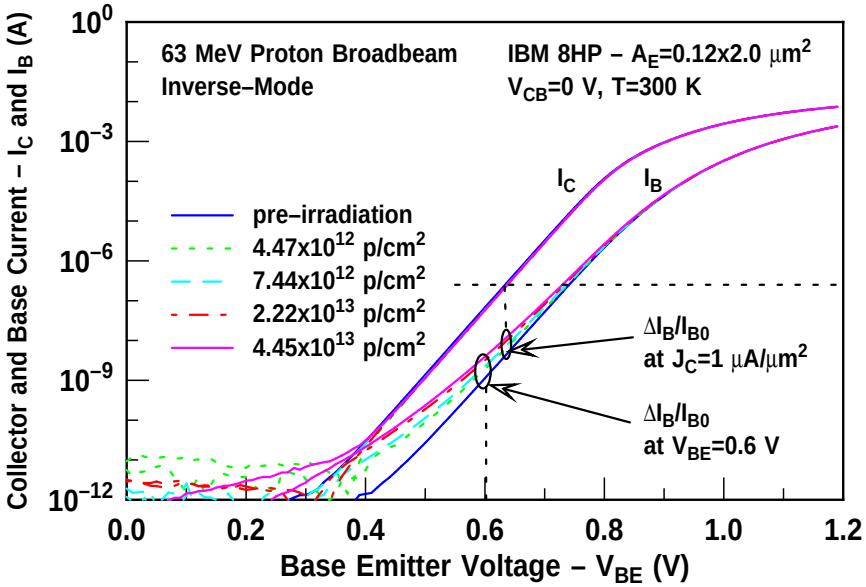

Figure 6: Inverse-mode Gummel characteristics of 3$^{\text{rd}}$-generation HBTs irradiated with 63 MeV protons to a cumulative fluence of 4.45×10^{13} p/cm^2.

Calibrated DESSIS 2-D TCAD simulations were used to qualitatively demonstrate the relationship between the forward- and inverse-mode ΔI_B and the carrier recombination rates near the BE spacer and STI, respectively. The pre- and post-irradiation recombination contours are illustrated in Figures 7 and 8 for transistor operation in the forward and inverse mode, respectively.

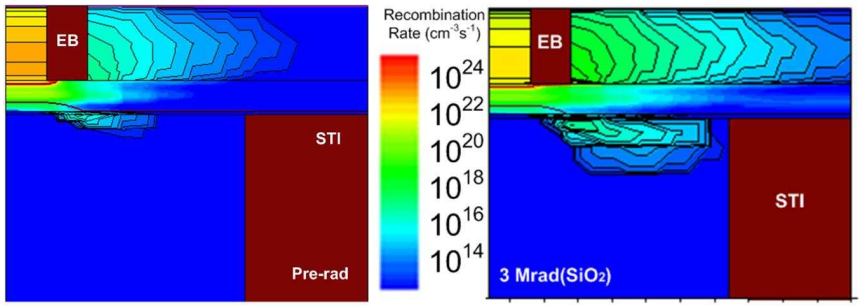

Figure 7: Pre- and post-irradiation recombination contours in the forward mode for 3rd-generation HBTs irradiated with 63 MeV protons to a cumulative fluence of 4.45×10^{13} p/cm^2.

The post-irradiation Gummel characteristics in the forward and inverse mode were simulated by the addition of positive oxide trapped charge in both the BE spacer and STI, respectively, and by the addition of interface traps in the corresponding Si/SiO_2 interfaces. Midgap traps, featuring electron and hole capture cross sections of 8×10^{-16} cm^2 were included in the simulations. Doping-dependent bulk SRH, surface SRH, and trap-assisted Auger recombination models were also implemented.

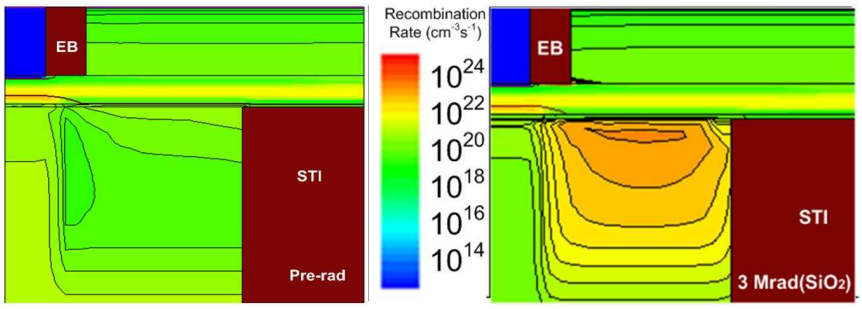

Figure 8: Pre- and post-irradiation recombination contours in the inverse mode for 3rd-generation HBTs irradiated with 63 MeV protons to a cumulative fluence of 4.45×10^{13} p/cm^2.

The simulated post-irradiation Gummel characteristics in the forward and inverse mode were matched to the corresponding transistor measurements after a cumulative dose of 3

Mrad(SiO_2). In the forward mode, the peak recombination rate is located near the BE spacer and is determined by the interface traps at this Si/SiO_2 interface. Conversely, in the inverse mode, the peak recombination rate is located near the STI. Finally, in both modes there is a significant increase in the peak recombination rate after irradiation.

3.4.2 Common-Emitter Output Characteristics

In Figure 9, the common-emitter output characteristics of a 3rd-generation HBT are illustrated for 63 MeV proton irradiation to a cumulative dose of 6 Mrad(SiO_2). This measurement is made by grounding the emitter terminal (V_E=0 V), forcing a current into the base, and sweeping the collector-emitter voltage from V_{CE}=0 V to 2.25 V. The two output traces illustrated in Figure 9 are representative of transistor operation at high injection, for which I_B=10 μA, and at low injection, for which I_B=1 nA.

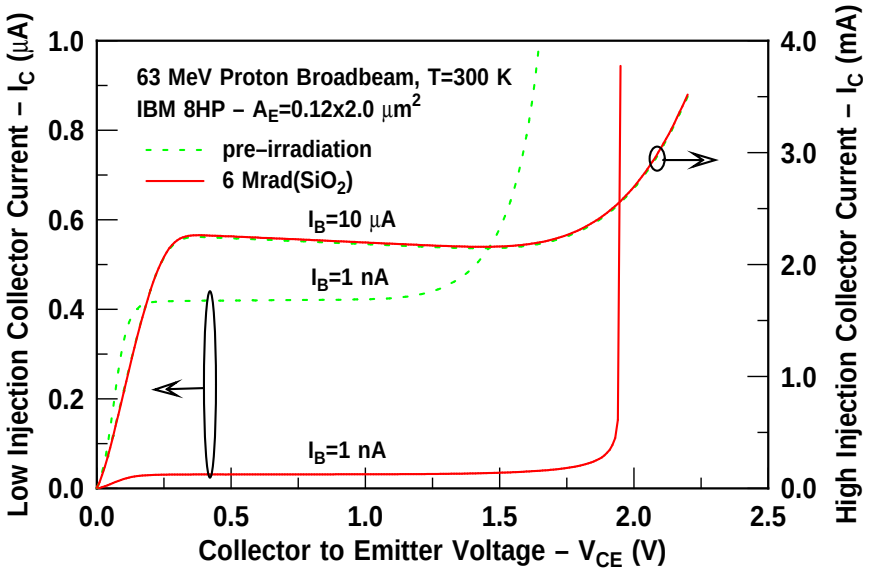

Figure 9: Forced-I_B output characteristics at high and low injection for a 3rd-generation HBT irradiated with 63 MeV protons to a cumulative dose of 6 Mrad(SiO_2).

For high injection, neither the common-emitter breakdown voltage (BV_{CE}) nor I_C changes, but for low injection, there is a decrease of 80% in I_C and an increase of 30% in BV_{CE}. It is important to note that the BV_{CE} defined here is different from the more-common BV_{CE0}. BV_{CE0} is defined as the common-emitter breakdown voltage for an open base, but if a current is forced into the base, as is the case in this measurement, then the

breakdown illustrated in Figure 9 is defined as BV_{CE} and is typically greater than BV_{CE0}.

The reduction in the low-injection I_C is a result of the radiation-induced ΔI_B, which enables the pre-irradiation I_B values to be achieved at a smaller V_{BE} and I_C according to (61). In BJTs, the breakdown observed in the common-emitter output characteristics may be caused by either junction punch-through or avalanche multiplication [29]. If junction punch-through is responsible for the breakdown, then the dependence of BV_{CE} on V_{CB} is determined by carrier recombination in the neutral base (NBR). This NBR dependence is result of the fact that the base is lightly doped when compared to either the collector or emitter ($N_{DC} \ggg N_{AB}$ and $N_{DE} \ggg N_{AB}$). Therefore, when the BE and BC junctions are reverse biased, both the BE and BC depletion regions extend further into the base than into either the collector or emitter. The NBR component of the base current (J_{B3} in (65)), is affected by perturbations in the charge stored in the neutral base (Q_B in (65)), the radiation-induced dopant deactivation in the base, and the presence of a radiation-induced image charge at the Si/SiO_2 interfaces near the neutral base.

Avalanche multiplication is the second possible cause of the common-emitter breakdown shown in Figure 9. In the forward mode, electrons are injected from the emitter into the base and create additional e-h pairs via impact ionization near the BC junction, which occurs even if V_{CB} is much greater than BV_{CB0}. The impact-ionized electrons and emitter-injected electrons are then transported together into the collector, while the impact-ionized holes are swept into the base. When the transistor in the common-emitter configuration, I_B is determined externally, and the impact-ionized holes are injected into the base to achieve carrier balance. Once in the base, some of these holes are injected back into the emitter where they trigger additional electron injection from the emitter into the base. As a result of β-induced current amplification, the number of electrons injected into the base is larger than the number of injected into the emitter. This process is regenerative, and each e-h pair that is created in the BC depletion region contributes to carrier multiplication, which causes I_C to rapidly increase at V_{CE} values far below BV_{CE0}.

3.4.3 Avalanche Multiplication

The avalanche multiplication factor (M) is used to describe the difference between the collector current entering ($I_{C,in}$) and leaving ($I_{C,out}$) the BC depletion region. M can be written as [6]

$$M = \frac{I_{C,out}}{I_{C,in}}. \tag{67}$$

To emphasize the net increase in I_C, it is more common to express avalanche multiplication using the $M-1$ factor. $M-1$ is measured by configuring the transistor in common-base mode, forcing a current into the emitter (I_E), sweeping the collector-base voltage from V_{CB}=0 V to 4 V, and measuring I_C and V_{BE}. This fixed-I_E measurement technique avoids self-heating and thermal runaway and is thus a safer alternative to the fixed-V_{BE} measurement technique [246]. Using the fixed-I_E technique, $I_{C,in}$ can be written as [6]

$$I_{C,in} = I_E - I_B\left(V_{CB}\right)\Big|_{V_{CB}=0\text{ V}}, \tag{68}$$

which then allows for $M-1$ to be calculated according to [6]

$$M - 1 = \frac{I_C}{I_E - I_B\left(V_{CB}\right)\Big|_{V_{CB}=0\text{ V}}} - 1, \tag{69}$$

where $I_B\left(V_{CB}\right)\Big|_{V_{CB}=0\text{ V}}$ is the value of I_B at V_{CB}=0 V for the value of V_{BE} observed during the $M-1$ measurement. The pre- and post-irradiation $M-1$ factors for 1$^{\text{st}}$- and 3$^{\text{rd}}$-generation HBTs are illustrated in Figure 10.

The avalanche multiplication in 3$^{\text{rd}}$-generation HBTs is significantly larger than in 1$^{\text{st}}$-generation HBTs because of the increases in both N_{DC} and the electric field of the BC junction [247]. Furthermore, a decrease in $M-1$ is observed in both technology platforms at 6 Mrad(SiO_2). This decrease is driven by the radiation-induced reduction in β, which lessens the regenerative nature of the carrier multiplication processes and results in a larger V_{CB} being required to achieve the same $M-1$ and BV_{CE}.

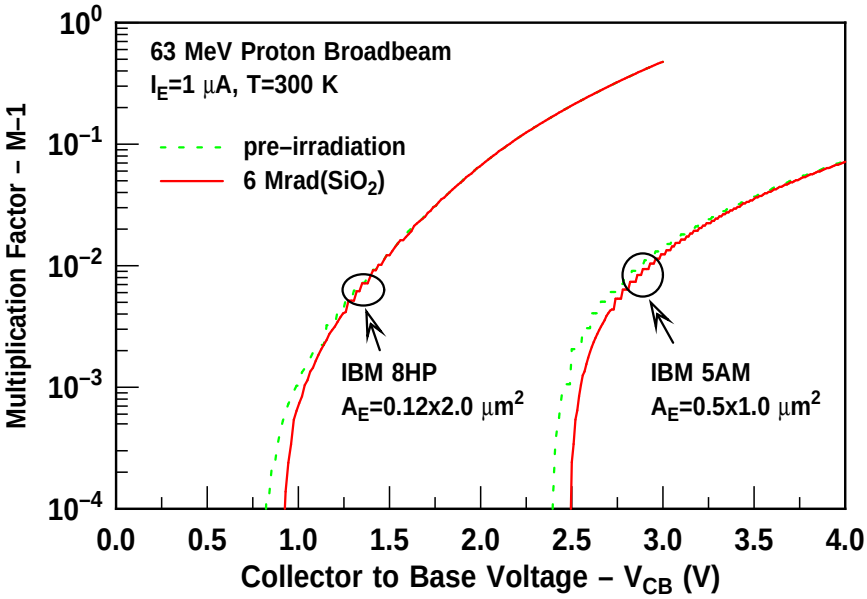

Figure 10: Pre- and post-irradiation $M-1$ vs. V_{CB} for 1st- and 3rd-generation HBTs irradiated with 63 MeV protons to a cumulative dose of 6 Mrad(SiO_2).

3.4.4 Neutral Base Recombination

To investigate the contribution of recombination in the neutral base to the overall radiation-induced ΔI_B, an independent NBR measurement was made. In measuring NBR, the transistor is configured in the common-base mode, a current is forced into the emitter, and the collector-base voltage swept from V_{CB}=0 V to 4 V. If NBR is negligible, then the minority-carrier diffusion length for electrons in the base is significantly greater than the base width ($L_{nB} \ggg W_B$). Therefore, there is no change in I_B when W_B decreases as V_{CB} is increased. Conversely, if NBR is significant, then L_{nB} is comparable to W_B and any perturbations in V_{CB} that cause a reduction in W_B will result in a reduction in the contribution of the overall NBR component (J_{B3} in (65)). J_{B3} can also be written as [6]

$$J_{B3} = \frac{q}{\tau_{nb}} \left\{ \frac{C_1 \left[e^{m_1 W_B} \right] - 1}{m_1} + \frac{C_2 \left[e^{m_2 W_b} \right] - 1}{m_2} + \frac{(1+m_0)\left[n_{b0}\left(W_b\right) - n_{b0}\left(0\right) \right]}{\triangle E_{g,Ge}\left(grade\right)/k_B T W_B} \right\}, \quad (70)$$

where C_1, C_2, $m_1(x)$, $m_2(x)$, $n_{b0}(x)$, and $m_0(x)$ are all terms that are derived in the solution of a second-order differential equation obtained from the current-continuity and drift-diffusion transport equations of the position-dependent carrier concentration in the base. These terms are all related to $\Delta E_{g,Ge}(grade)$, W_B, and L_{nb}.

In Figure 11, the pre- and post-irradiation normalized I_B are plotted as a function of V_{CB} for 1st- and 3rd-generation HBTs biased at I_E=1 μA. In Figure 12, the pre- and post-irradiation normalized I_B are plotted again as a function of V_{CB} with the x-axes and y-axes expanded to illustrate base current reversal.

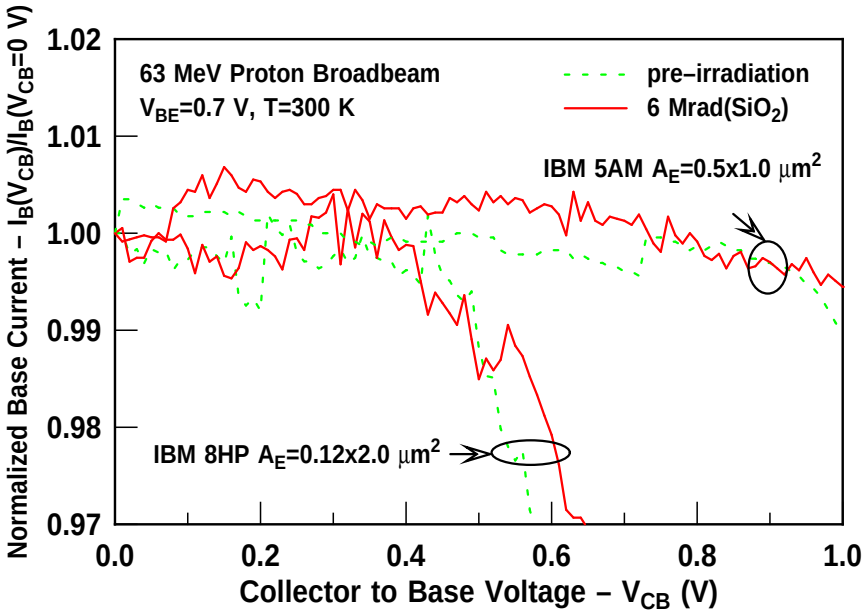

Figure 11: Pre- and post-irradiation $\frac{I_B(V_{CB})}{I_B(V_{CB}=0.7\ \mathrm{V})}\big|_{V_{BE}=0.7\ \mathrm{V}}$ vs. V_{CB} for 1st- and 3rd-generation HBTs irradiated with 63 MeV protons to a cumulative dose of 6 Mrad(SiO_2).

In the common-emitter configuration, the increase in I_C as a result of avalanche multiplication is accompanied by a reduction in I_B. This reduction in I_B continues until I_B eventually changes polarity and becomes negative. The bias condition at which this occurs is known as the "base current reversal point" and is determined by [6]

$$\beta\,\big|_{V_{CB}=0\ V} \times F_{Early} \times (M-1) = 1, \tag{71}$$

where F_{Early} is the Early effect factor, which can be written as [6]

$$F_{Early} = \frac{I_C\,(V_{CB}) - \triangle I_B}{I_C\,(V_{CB}=0\ V)}. \tag{72}$$

F_{Early} is used in conjunction with the Early voltage (V_A) to describe the Early effect [247][248]. Therefore, the V_{CB} at which I_B becomes negative is indicative of the degree of avalanche multiplication in the transistor.

As shown in Figure 12, this voltage increases after 6 Mrad(SiO_2), which is consistent with the larger post-irradiation BV_{CE} shown in Figure 9. Up to a dose of 6 Mrad(SiO_2), NBR is negligible in both 1st- and 3^{rd}-generation HBTs, which implies that junction punch-through is not the cause of the common-emitter breakdown shown in Figure 9. Furthermore, the absence of an NBR component also indicates that if atomic displacement and dopant de-activation do occur in these 3rd-generation HBTs following 63 MeV proton irradiation, they are not strong enough to influence carrier recombination in the base.

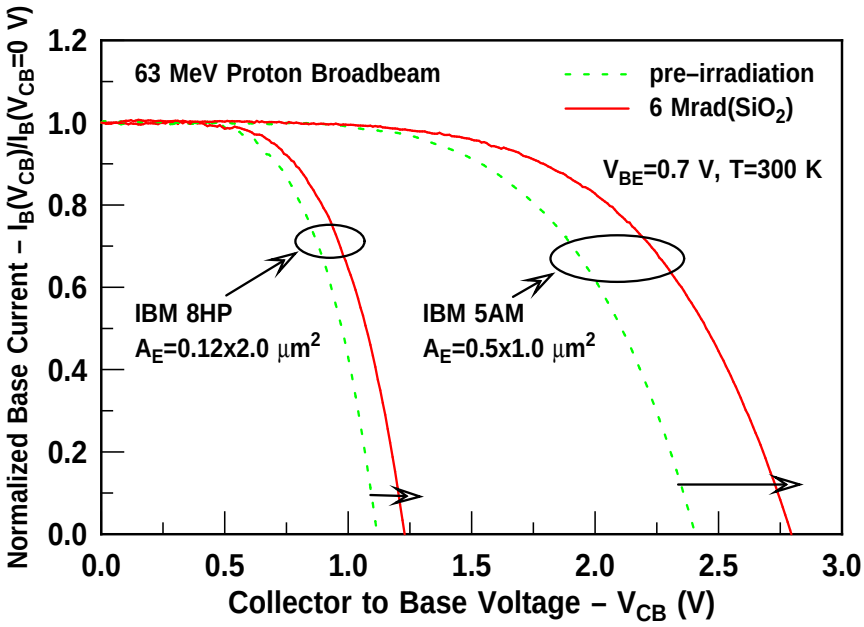

Figure 12: Figure 11 re-plotted with the x- and y-axes expanded to illustrate base current reversal in 1st- and 3rd-generation HBTs irradiated with 63 MeV protons to a cumulative dose of 6 Mrad(SiO_2).

3.4.5 Low-Frequency Noise

The nature of radiation-induced positive oxide trapped charge and Si/SiO_2 interface traps has been widely studied using measurements low-frequency ($1/f$) noise in MOSFETs [176][249]. In this section, the impact of 63 MeV proton irradiation on the $1/f$ noise of 3rd-generation SiGe HBTs is investigated. Transistors with an A_E of 0.12×1.0, 0.12×2.0, 0.12×4.0, and 0.12×8.0 μm^2 were packaged into 28-pin DIPs, irradiated with all terminals grounded, and an automatic noise measurement system, which is fully described in [250], was used to measure the voltage and current power spectral densities.

Transistor were biased using a custom-made voltage divider comprised of automated wire-round resistors connected between a 12 V battery and the transistor terminals. Battery power was used to minimize all external noise sources, and the transistors were configured in common-emitter mode with load resistors, R_S and R_L, connected in series to the base and collector terminals, respectively. An Agilent 35670A Dynamic Signal Analyzer (DSA) was used to measure the power spectral densities on the collector (S_{VC}) and base (S_{VB}) after amplification by an EGG preamplifier. Invoking the hybrid-π equivalent model allows S_{VC} and S_{VB} to be written as [251]

$$S_{VC} = \left(\frac{R_L R_S \beta}{R_S + r_\pi} \right)^2 S_{IB} \tag{73}$$

and

$$S_{VB} = \left(\frac{R_S r_\pi}{R_S + r_\pi} \right)^2 S_{IB}, \tag{74}$$

where $\beta = \frac{dI_C}{dI_B}$ is the dynamic current gain, $r_\pi = \frac{dV_{BE}}{dI_B}$ is the base-emitter input impedance, and S_{IB} is the base-current power spectral density.

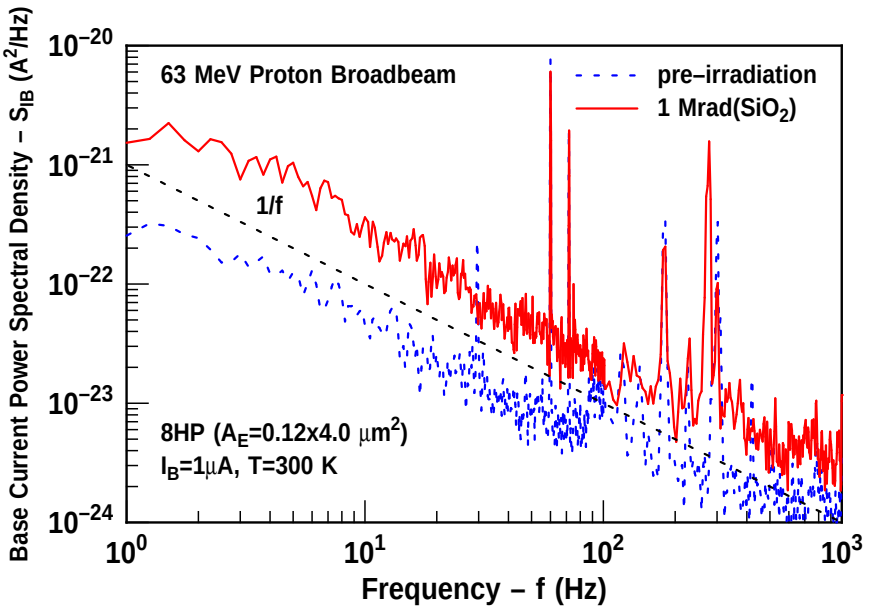

Figure 13: Pre- and post-irradiation S_{I_B} at I_B=1 μA vs. frequency for a 3$^{\text{rd}}$-generation HBT irradiated with 63 MeV protons to a cumulative dose of 1 Mrad(SiO_2).

The pre- and post-irradiation S_{I_B} ($S_{I_B,pre}$ and $S_{I_B,post}$) are extracted at I_B=1 μA and plotted as a function of frequency in Figure 13. At a dose of 1 Mrad(SiO_2), $S_{I_B,post}$ is

still proportional to $1/f$ and is 700% larger than $S_{I_{B,pre}}$. Since S_{VC} and S_{VB} are highly coherent, the S_{IB} values extracted from (73) and (80) are identical, which means that S_{IB} is the dominant noise source [250]. The pre-irradiation S_{I_B} ($S_{I_{B,pre}}$) is expressed as [252]

$$S_{I_{B,pre}} = \frac{K I_B^{\alpha_H}}{A_E f}, \tag{75}$$

where K is a technology-dependent fitting parameter and α_H is the Hooge parameter [253], which can be used to determine the origin of the observed $1/f$ noise.

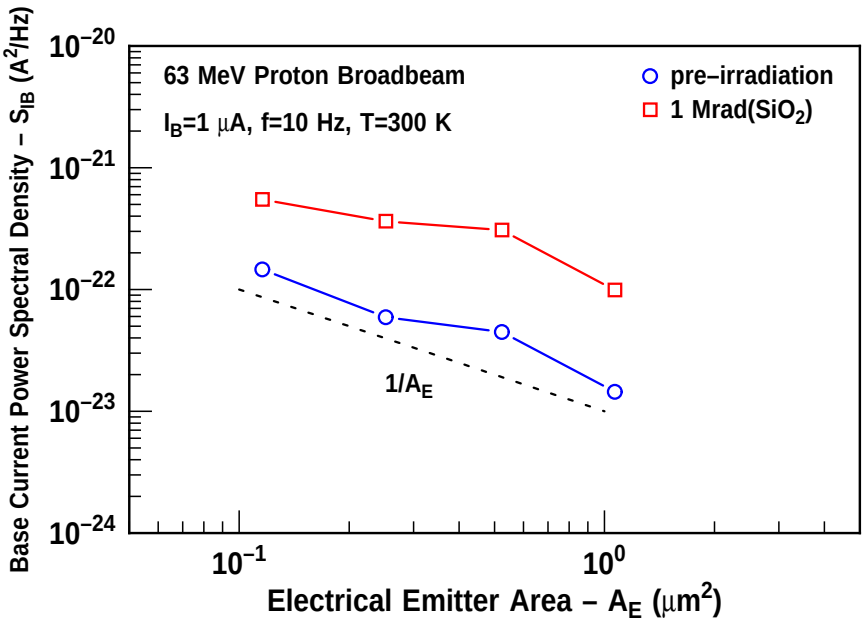

Figure 14: Pre- and post-irradiation S_{I_B} at I_B=1 μA and f=10 Hz vs. A_E for 3$^{\text{rd}}$-generation HBTs irradiated with 63 MeV protons to a cumulative dose of 1 Mrad(SiO_2).

The $S_{I_{B,pre}}$ and $S_{I_{B,post}}$ of transistors with the aforementioned A_E values are extracted at f=10 Hz and I_B=1 μA and plotted as a function of A_E in Figure 14.Again, at 1 Mrad(SiO_2), $S_{I_{B,post}}$ is proportional to $1/A_E$ and is 700% larger than $S_{I_{B,pre}}$. Finally, $S_{I_{B,pre}}$ and $S_{I_{B,post}}$ are extracted at f=10 Hz and plotted as a function of I_B in Figure 15.

At 1 Mrad(SiO_2), the dependence of $S_{I_{B,post}}$ on I_B changes from a closer-to-I_B dependence to a closer-to-I_B^2 dependence. As illustrated in Figure 15, the pre-irradiation value of α_H is close to two, which indicates that fluctuations in the carrier density are heavily involved in the noise response [254][255]. The source of these fluctuations is rooted in the continuous trapping and de-trapping of carriers facilitated by defects in the bulk SiO_2 and

Si/SiO_2 interfaces [256]. Near the BE junction, the spreading of the depletion region, which is also referred to as the space charge region (SCR), after irradiation results in more interaction between the BE junction and interface traps associated with the BE spacer. Therefore, $S_{I_B,post}$ is a weighted combination of the $S_{I_B,pre}$ component and the $S_{I_B,SCR}$ component.

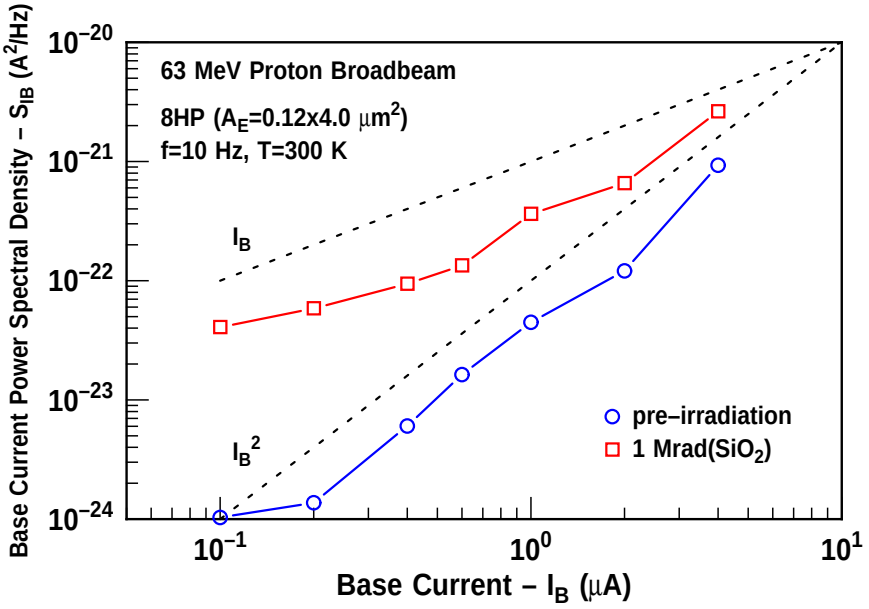

Figure 15: Pre- and post-irradiation S_{I_B} at f=10 Hz vs. I_B for a 3rd-generation HBT irradiated with 63 MeV protons to a cumulative dose of 1 Mrad(SiO_2).

Since the I_B component resulting from the interaction of the BE SCR with the Si/SiO_2 interface ($I_{B,SCR}$) is dependent on the perimeter of the emitter (P_E), $I_{B,SCR}$ may be written as [252]

$$I_{B,SCR} \propto \exp\left(\frac{qV_{BE}}{2k_BT}\right) P_E N_T, \tag{76}$$

where N_T is the radiation-induced surface trap density. The noise contribution from $I_{B,SCR}$ ($S_{I_B,SCR}$) can then written as [257]-[259]

$$S_{I_{B,SCR}} = I_{B,SCR}^2 \left(\frac{\alpha_H}{fN_T}\right). \tag{77}$$

Furthermore, $I_{B,SCR}$ can be expressed in terms of I_B by writing [252]

$$I_B \propto \exp\left(\frac{qV_{BE}}{k_BT}\right) A_E. \tag{78}$$

Therefore, by combining (76) and (78), $S_{I_B,SCR}$ can be expressed as [252]

$$S_{I_{B,SCR}} = CI_B N_T \left(\frac{\alpha_H P_E}{fA_E}\right), \tag{79}$$

where C is a bias- and geometry-dependent constant. Finally, $S_{I_{B,post}}$ can be expressed as the sum of $S_{I_{B,pre}}$ and $S_{I_{B,SCR}}$ by writing [252]

$$S_{I_{B,post}} = S_{I_{B,pre}} + S_{I_{B,SCR}} = \frac{K}{A_E} I_B^2 \frac{1}{f} + C I_B N_T \frac{P}{A_E} \frac{\alpha_H}{f}, \tag{80}$$

where the radiation-dependent variation in the I_B dependence of $S_{I_{B,post}}$ is clearly accounted for by an increase in the contribution of the second term as N_T increases after irradiation.

3.4.6 Mixed-Mode Electrical Stress

Depending on the circuit application, the radiation-induced ΔI_B may be a reliability concern for SiGe HBTs. Similar ΔI_B phenomena in this technology platform have been identified using reverse-bias base-emitter stress [260], high forward current density stress [261][262], and mixed-mode stress [263]. The terminology used to describe the stress technique is determined by the values of emitter current density and base-collector voltage that are applied during the stressing sequence. To be sure, a very complicated damage spectrum exists for HBTs stressed at J_E values ranging from 10^{-8} μA/μm^2 to 10^{-1} μA/μm^2 and at V_{BC} values ranging from 0 V to 10 V. Interestingly, at certain J_E and V_{BC} values both the stress- and radiation-induced ΔI_B may be even annealed [264].

Stress-induced ΔI_B in SiGe HBTs is caused by hot-carrier-induced degradation [265], and among the many proposed mechanisms, theories invoking the "lucky electron" model are quite popular. In the lucky electron model, a hot electron with kinetic energy greater than the trap creation energy (2.3 eV) interacts with the BE spacer or STI and generates traps along the corresponding Si/SiO_2 interfaces [266][267]. The plausibility of the lucky electron model is supported both by the fact that the mean path length of hot electrons is on the same order of magnitude as the distance between the BE spacer and STI and by experimental observations of large variations in the stress-induced ΔI_B as a function of the STI-to-SIC distance.

In this section, the influence of mixed-mode electrical stress on the proton response of 3$^{\text{rd}}$-generation SiGe HBTs is investigated. Transistors with an A_E of 0.12×4.0 μm^2 were irradiated to a cumulative dose of 1 Mrad(SiO_2) and subsequently exposed to a mixed-mode

stress sequence at J_E=-40 μA/μm^2 and V_{CB}=3 V. The forward-mode Gummel characteristics were measured during the stress sequence at time intervals ranging from 10^{-3} s to 3×10^3 s. For a second set of transistors, the irradiation and stressing sequences were reversed. The normalized excess base current, extracted at V_{BE}=0.6 V $\left(\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}\right)$, is used as the figure of merit to compare the stress- and radiation-induced damage. In Figure 16, $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ is plotted as a function of dose for two transistors. The first was stressed up to 3×10^3 s before irradiation and the second was not stressed.

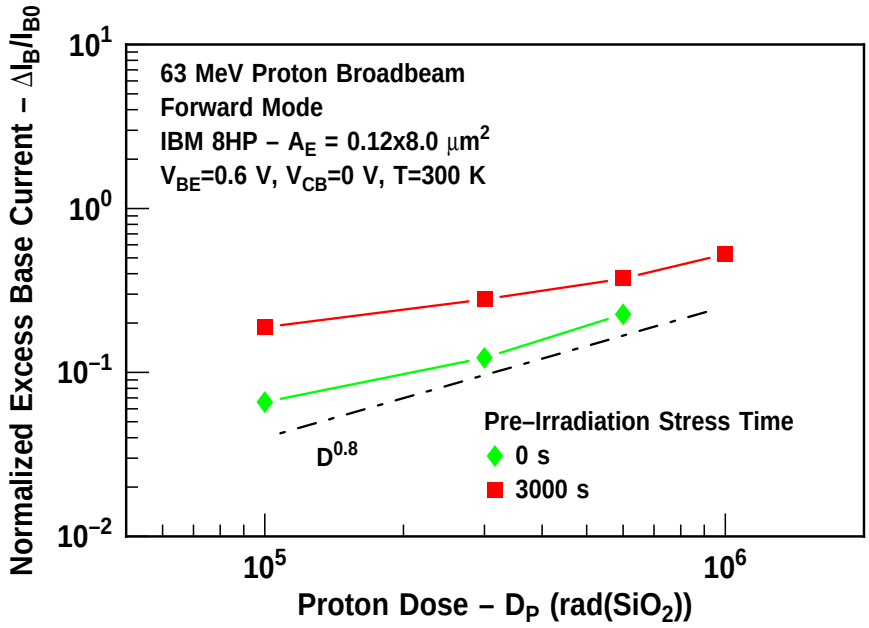

Figure 16: Forward-mode $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ vs. 63 MeV proton dose for 3$^{\text{rd}}$-generation HBTs before and after 3000 s of mixed-mode electrical stress at J_E=-40 μA/μm^2 and V_{CB}=3 V.

In Figure 17, $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ is plotted as a function of the cumulative mixed-mode stress time for two transistors. The first was irradiated to a dose of 1 Mrad(SiO$_2$) before stress and the second was not irradiated. As shown in Figure 16, $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ has a near-linear dose dependence in both the pre- and post-stressed transistors. After the first incremental dose of 100 krad(SiO$_2$), $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ is 186% larger in the post-stressed device. However, as the dose is increased, the difference between the $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ values in the pre- and post-stressed transistors decreases significantly, which indicates that it is the radiation-induced interface trap formation that dominates the combined response.

In Figure 17, $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ also has a linear dependence on the cumulative mixed-mode

stress time for both the pre- and post-irradiated transistors at low stress times. After 10^0 s, $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ for the post-irradiated transistor saturates at a value close to one, while $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ for the pre-irradiated transistor continues to increase. Similar results were obtained for the inverse-mode $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ across transistors of varying A_E.

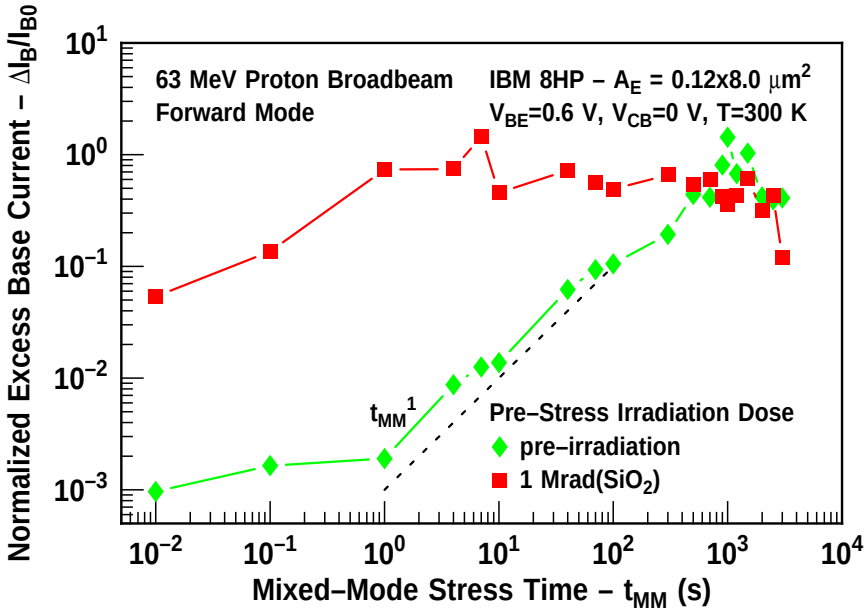

Figure 17: Forward-mode $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ vs. mixed-mode stress time for 3$^{\text{rd}}$-generation HBTs before and after irradiated with 63 MeV protons to a cumulative dose of 1 Mrad(SiO_2).

3.4.7 Transistor Bias

The initial charge yield is a strong function of the oxide electric field (E_{OX}) [268]. In MOS devices, E_{OX} is well defined between the gate electrode, which lies directly on top of the gate oxide, and the channel region, which lies directly under the gate oxide. Conversely, in vertical BJTs there is no planar arrangement of the collector, base, or emitter electrodes in relation to the BE spacer or STI, as illustrated for 1$^{\text{st}}$- and 3$^{\text{rd}}$-generation HBTs in Figures 2 and 3, respectively. This electrode arrangement means that for these HBTs, electric field lines are fringing inside the oxide, and the radiation-induced degradation is less dependent on E_{OX} than for MOSFETs [269][270]. In Figure 18, the forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ are plotted as a function of dose for transistors biased with either all terminals grounded (V_C=V_B=V_E=V_S=0 V) or under "stable bias", in which the

BE junction is forward biased (V_C=0.5 V, V_B=V_S=0 V, and V_E=-0.8 V). At the first incremental dose of 130 krad(SiO_2), both the forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ are 117% larger for the transistor irradiated under a stable bias. This result is consistent with an increase in charge yield at larger E_{ox}. As the dose is increased, the differences in the radiation response as a function of transistor bias are negligible.

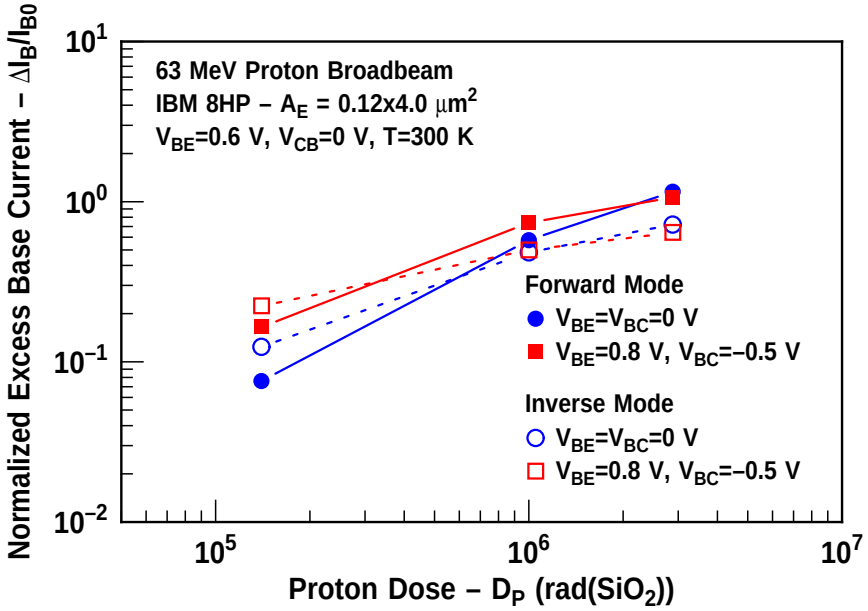

Figure 18: Forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ vs. 63 MeV proton dose for 3rd-generation HBTs biased with all terminals grounded and in a stable bias configuration.

3.4.8 High-Temperature Annealing

The isochronal and isothermal annealing characteristics of 3rd-generation SiGe HBTs with an A_E of 0.12×4.0 μm^2 are illustrated in Figures 19 and 20, respectively. Transistors were irradiated to a cumulative dose of 6 Mrad(SiO_2), and high-temperature annealing was performed in a forming gas (N_2H_2) ambient using an AET Rapid Thermal Annealing system. Before each anneal step, the chamber was purged with 2 sccm of N_2 for two minutes. The ambient was then switched to N_2H_2, and the temperature was ramped to the desired value at a rate of 1.67 K/s. At the end of each anneal step, the transistors were left to cool to 273 K before they were removed from the chamber and measured at room temperature. Isochronal annealing was performed in a sequence of steps, each using the same anneal

time (t_A) of 300 s and variable anneal temperatures (T_A) ranging from 273 K to 573 K. Isothermal annealing was also performed in a sequence of steps, using T_A=300 or 573 K, and t_A ranging from 10^1 s to 10^6 s.

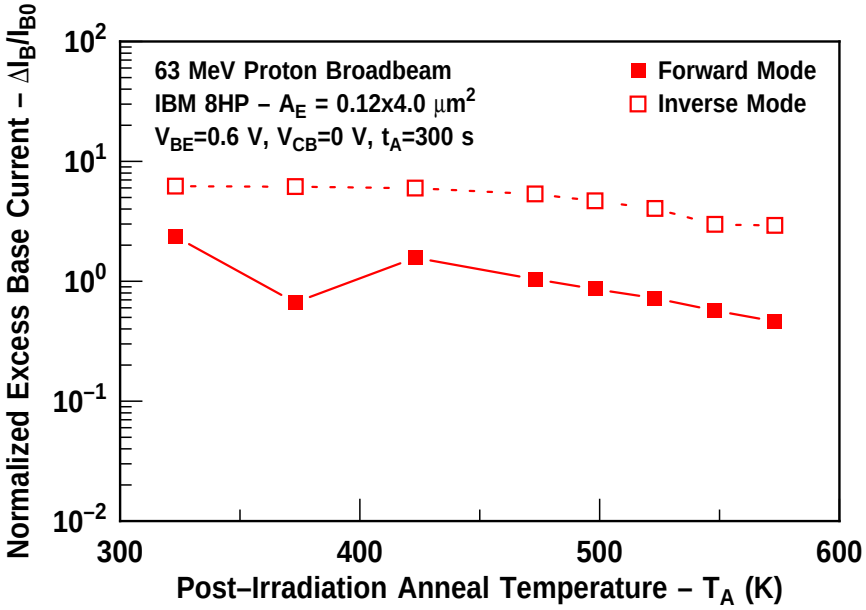

Figure 19: Forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ vs. anneal temperature for 300 s isochronal anneals of 3$^{\text{rd}}$-generation HBTs irradiated with 63 MeV protons to a cumulative dose of 6 Mrad(SiO_2).

Both the forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ gradually decrease as a function of T_A, as shown in Figure 19. The slope of curves in Figure 19 is determined by t_A, the ambient, and the distribution of Si/SiO_2 interface traps and bulk oxide traps. Si/SiO_2 interface traps are annealed between 273 K and 473 K, whereas positive oxide trapped charge is annealed between 423 K and 573 K [16]. In Figure 19, $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ is plotted as a function of t_A at 300 K and 573 K. At 300 K, neither the forward- nor the inverse-mode $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ decreases after 10^6 s. However, as the temperature is increased to 573 K, there is significant recovery after just 10^3 s. Additionally, the inverse-mode $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ recovers more slowly than the forward-mode $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$, regardless of the anneal time or temperature. These results are indicative of the fact that process variations in the fabrication of bulk oxides result in different levels of molecular H_2 being incorporated into the films. This phenomenon influences the buildup of radiation-induced oxide trapped

charge and interface traps, as shown in [271].

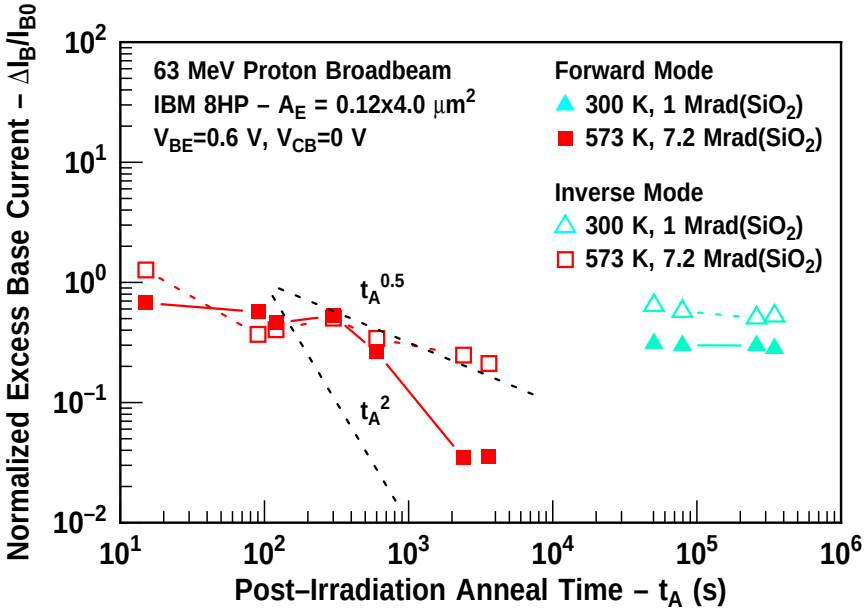

Figure 20: Forward- and inverse-mode $\frac{\Delta I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ vs. cumulative anneal time for 300 K and 573 K isothermal anneals of 3$^{\text{rd}}$-generation HBTs irradiated with 63 MeV protons to a cumulative dose of 6 Mrad(SiO_2).

3.5 The Effects of Technology Scaling on Medium-Energy Proton-Induced Degradation

3.5.1 *dc* Performance Degradation

In this section, the impact of 63 MeV proton irradiation on the forward- and inverse-mode ΔI_B of 1$^{\text{st}}$- through 4$^{\text{th}}$-generation SiGe HBTs is compared. As depicted in Figures 4 and 6, there are several figures of merit that may be used to facilitate this comparison. These include $\frac{\Delta I_B}{I_{B0}}$ at fixed-V_{BE}, $\frac{\Delta I_B}{I_{B0}}$ at fixed-J_C, ΔJ_B at fixed-V_{BE}, and ΔJ_B at fixed-J_C. A comparison of the pre-irradiation transistor performance as a function of technology generation is a logical prerequisite to any investigation into the impact of technology scaling on the observed proton response. The pre-irradiation forward- and inverse-mode Gummel characteristics of 1$^{\text{st}}$- through 4$^{\text{th}}$-generation HBTs are illustrated in Figures 21 and 22,respectively. The fixed-V_{BE} (V_{BE}=0.6 V) and fixed-J_C (J_C=1 μA/μA) extraction points are highlighted in both figures. It is important to note that the transistors chosen for the comparison of scaling effects all had similar A_E values, as shown in Table 3.

The implications of technology scaling on the forward-mode J_C and J_B, as shown in Figure 21, are now considered. In the forward mode, both J_C and J_B for 2nd-generation HBTs are significantly larger than for 1st-generation HBTs, but the pre-irradiation forward-mode J_C and J_B of 2nd- and 3rd-generation HBTs overlay. Furthermore, an additional enhancement in the forward-mode J_C and J_B is observed in going from the 3rd- to 4th-generation technology platform.

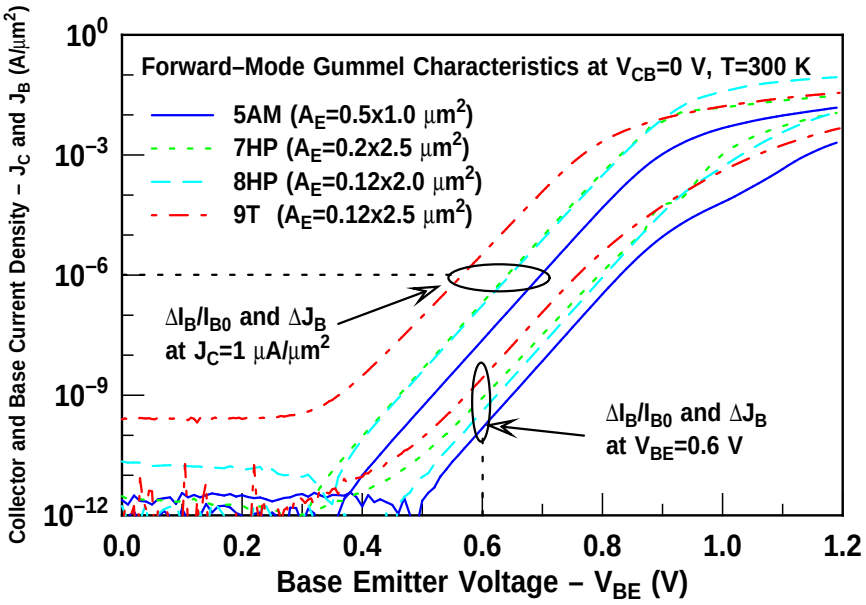

Figure 21: Forward-mode Gummel characteristics of 1st- through 4th-generation HBTs.

The increases in the forward-mode J_C as a function of technology scaling are driven by reductions in the base *Gummel number* (G_B), which result from the scaling-driven reductions in the base width (W_B) in the integral expression for G_B given by [272]

$$G_B = \int_0^{W_B} \left(\frac{n_i^2}{n_{iB}^2}\right) \left(\frac{N_{AB}}{D_{nB}}\right) dx, \tag{81}$$

where n_i is the intrinsic carrier density, n_{iB} is the Ge-induced intrinsic carrier density in the base (as defined in (43)), N_{AB} is the acceptor doping in the base, and D_{nB} is the diffusivity constant of electrons in the base. Similarly, the increases in the forward-mode J_B are driven by reductions in the emitter Gummel number (G_E), which can be expressed as [272]

$$G_E = \int_0^{-W_E'} \left(\frac{n_i}{n_{iE}}\right)^2 \left(\frac{N_{DE}}{D_{pE}}\right) dx + \frac{n_i^2 N_{DE}\left(-W_E'\right) W_{Epoly}}{n_{iE}^2\left(-W_E'\right) D_{pEpoly}}, \tag{82}$$

where W'_E is the short-emitter width, n_{iE} is the doping-induced intrinsic carrier density in the emitter, N_{DE} is the donor doping in the emitter, D_{pE} is the diffusivity of holes in the short emitter, D_{pEpoly} is the diffusivity of holes in the polysilicon emitter, and W_{Epoly} is the width of the polysilicon emitter. If the conditions of uniform doping are invoked, then the forward-mode J_C and J_B may be written as [272]

$$J_C = \frac{qn_{iB}^2}{G_B} \exp\left(\frac{qV_{BE}}{k_B T}\right) \tag{83}$$

and

$$J_B = \frac{qn_{iE}^2}{G_E} \exp\left(\frac{qV_{BE}}{k_B T}\right), \tag{84}$$

where G_B and G_E can be approximated as $\frac{N_{AB}W_B}{D_{nB}}$ and $\frac{N_{DE}L_{pE}}{D_{pE}}$, respectively.

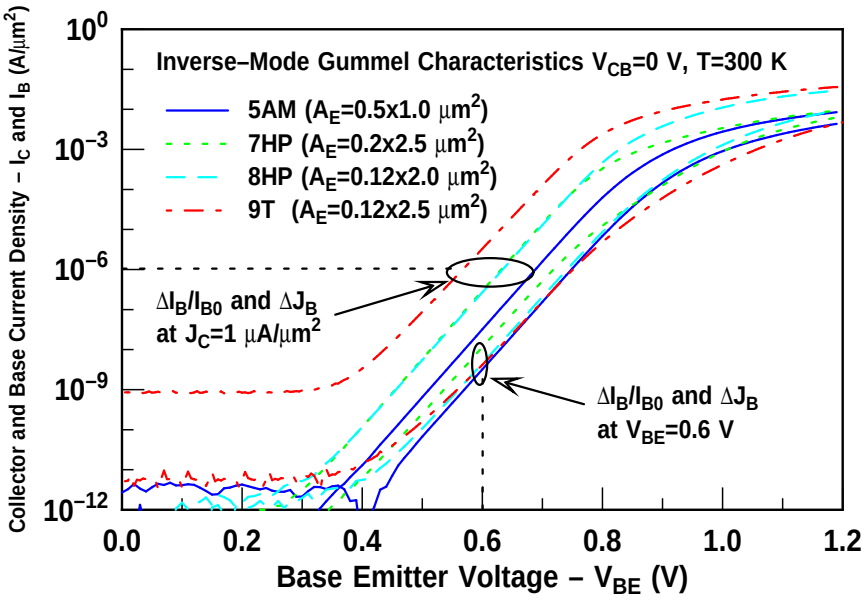

Figure 22: Inverse-mode Gummel characteristics of 1st- through 4th-generation HBTs.

The implications of technology scaling on the inverse-mode J_C and J_B, as shown in Figure 22, are now considered. Scaling-driven increases in f_T and f_{max} are realized by increasing N_{DC}, which delays the onset of high injection barrier effects [273]. Therefore, although a reduction in the inverse-mode J_B with scaling should be expected, a comparison of 1st- and 2nd-generation HBTs indicates a larger inverse-mode J_B for 2nd-generation HBTs. As expected, the inverse-mode J_C increases as a result of the reduction in W_B and the increase in N_{DC}. Unlike J_C, the inverse-mode J_B is dominated by neither A_E nor N_{DC}

but by the STI-to-SIC distance [244]. Although the inverse-mode J_C for 2nd- and 3rd-generation HBTs overlay, the 3rd-generation inverse-mode J_B is significantly lower because of the raised-extrinsic-base structure, which is used to remove the highly doped p-type base from the vicinity of the physical collector [244]. Finally, the vertical scaling that was utilized in the realization of 4th-generation HBTs results in an increased inverse-mode J_C and no change in the inverse-mode J_B.

Table 3: Selected geometries for 1st- through 4th-generation HBTs.

Figure of Merit	1st(5HP)[231]	2nd(7HP)[232]	3rd(8HP)[233]	4th(9T) [234]
Drawn A_E	0.50 μm^2	0.50 μm^2	0.24 μm^2	0.30 μm^2
Electrical A_E	0.30 μm^2	0.56 μm^2	0.25 μm^2	
Drawn P_E	3.00 μm	5.40 μm	4.24 μm	5.24 μm
Electrical P_E	2.21 μm	5.44 μm	3.92 μm	
Drawn P_E/A_E	6.00 1/μm	10.80 1/μm	17.67 1/μm	17.46 1/μm
Electrical P_E/A_E	6.85 1/μm	9.76 1/μm	15.56 1/μm	

The forward-mode ΔJ_B is extracted at V_{BE} = 0.6 V $\left(\triangle J_B\big|_{V_{BE}=0.6\text{ V}}\right)$ and at J_C = 1 μA/μm^2 $\left(\triangle J_B\big|_{J_C=1\ \mu\text{A}/\mu\text{m}^2}\right)$, and both of these quantities are plotted as a function of dose for 1st- through 4th-generation HBTs in Figure 23.

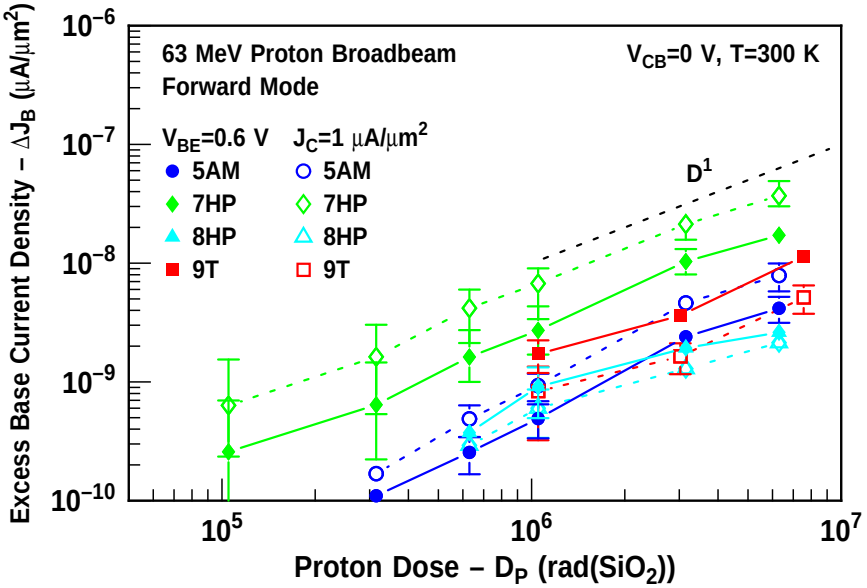

Figure 23: Forward-mode $\triangle J_B\big|_{V_{BE}=0.6\text{ V}}$ and $\triangle J_B\big|_{J_C=1\ \mu\text{A}/\mu\text{m}^2}$ vs. 63 MeV proton dose for 1st- through 4th-generation HBTs.

The corresponding forward-mode $\frac{\triangle I_B}{I_{B0}}$ is extracted at V_{BE}=0.6 V $\left(\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\ \mathrm{V}}\right)$ and at $J_C = 1\ \mu\mathrm{A}/\mu\mathrm{m}^2$ $\left(\frac{\triangle I_B}{I_{B0}}\big|_{J_C=1\ \mu\mathrm{A}/\mu\mathrm{m}^2}\right)$, and both of these quantities are plotted as a function of dose in Figure 24. The error bars on Figures 23 and 24, and similar plots thereafter, represent the maximum and minimum values of $\triangle J_B\big|_{V_{BE}=0.6\ \mathrm{V}}$ and $\triangle J_B\big|_{J_C=1\ \mu\mathrm{A}/\mu\mathrm{m}^2}$ for between two to four transistors.

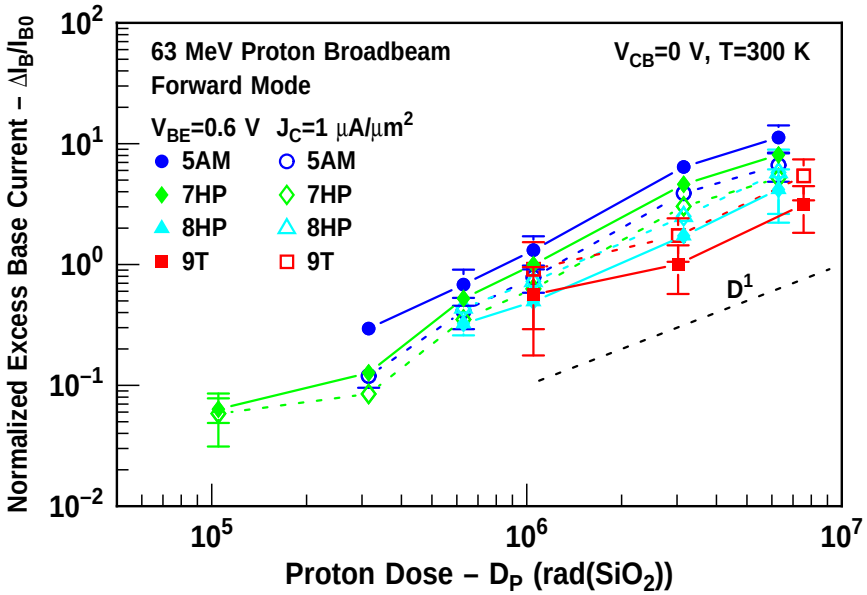

Figure 24: Forward-mode $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\ \mathrm{V}}$ and $\frac{\triangle I_B}{I_{B0}}\big|_{J_C=1\ \mu\mathrm{A}/\mu\mathrm{m}^2}$ vs. 63 MeV proton dose for 1$^{\mathrm{st}}$- through 4$^{\mathrm{th}}$-generation HBTs.

Proton-induced degradation in the forward mode is now compared as a function of technology scaling. In all technology platforms, the forward-mode $\triangle J_B\big|_{V_{BE}=0.6\ \mathrm{V}}$ and $\triangle J_B\big|_{J_C=1\ \mu\mathrm{A}/\mu\mathrm{m}^2}$ both exhibit a near-linear (D^1) dependence on dose. Depending on the value of the pre-irradiation J_B (J_{B0}) at the V_{BE} for which J_C=1 μA/μm, $\triangle J_B\big|_{J_C=1\ \mu\mathrm{A}/\mu\mathrm{m}^2}$ may be either greater or less than $\triangle J_B\big|_{V_{BE}=0.6\ \mathrm{V}}$. For the pre-irradiation characteristics of Figure 21, the forward-mode J_{B0} at the V_{BE} for which J_C=1 μA/μm is greater than 0.6 V for 1$^{\mathrm{st}}$- through 3$^{\mathrm{rd}}$-generation HBTs but less than 0.6 V for 4$^{\mathrm{th}}$-generation HBTs. This trend explains the fact that the forward-mode $\triangle J_B\big|_{V_{BE}=0.6\ \mathrm{V}}$ is less than the forward-mode $\triangle J_B\big|_{J_C=1\ \mu\mathrm{A}/\mu\mathrm{m}^2}$ for 1$^{\mathrm{st}}$- and 2$^{\mathrm{nd}}$-generation HBTs but greater than the forward-mode $\triangle J_B\big|_{J_C=1\ \mu\mathrm{A}/\mu\mathrm{m}^2}$ for 4$^{\mathrm{th}}$-generation HBTs.

Vertical profile scaling was employed in the migration from the 1st- to 2nd-generation HBTs and 3rd- to 4th-generation HBTs. In both cases, this scaling approach results in an increase in the forward-mode $\triangle J_B\big|_{V_{BE}=0.6\text{ V}}$ and $\triangle J_B\big|_{J_C=1\ \mu\text{A}/\mu\text{m}^2}$ for all doses. In going from the 1st- to 2nd-generation platform, at the final cumulative fluence of 6 Mrad(SiO_2), the forward-mode $\triangle J_B\big|_{V_{BE}=0.6\text{ V}}$ increases by 613% and the forward-mode $\triangle J_B\big|_{J_C=1\ \mu\text{A}/\mu\text{m}^2}$ increases by 712%. The corresponding increases in going from the 3rd- to 4th-generation platform are 420% and 186%, respectively. These increases are driven by the fact that vertical profile scaling moves the BE depletion region closer to the Si/SiO_2 interfaces of the BE spacer and STI. As previously stated, the implementation of the raised-extrinsic-base structure is done by moving the highly doped p-type base and BE depletion region away from the vicinity of the collector and the STI Si/SiO_2 interface. This new structure results in a significant reduction in both the forward-mode $\triangle J_B\big|_{V_{BE}=0.6\text{ V}}$ and $\triangle J_B\big|_{J_C=1\ \mu\text{A}/\mu\text{m}^2}$ by 93.1% and 97.4%, respectively. As shown in Figure 21, the use of vertical and lateral profile scaling translates into a forward-mode J_{B0} that monotonically increases with scaling and correlates to the monotonic decreases in the forward-mode $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ and $\frac{\triangle I_B}{I_{B0}}\big|_{J_C=1\ \mu\text{A}/\mu\text{m}^2}$ shown in Figure 24.

Proton-induced degradation in the inverse mode is now compared as a function of technology scaling. The inverse-mode $\triangle J_B\big|_{V_{BE}=0.6\text{ V}}$ and $\triangle J_B\big|_{J_C=1\ \mu\text{A}/\mu\text{m}^2}$, are plotted as a function of dose for 1st- through 4th-generation HBTs in Figure 25, and the corresponding inverse-mode $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ and $\frac{\triangle I_B}{I_{B0}}\big|_{J_C=1\ \mu\text{A}/\mu\text{m}^2}$ are plotted in Figure 26. The inverse-mode $\triangle J_B\big|_{V_{BE}=0.6\text{ V}}$ and $\triangle J_B\big|_{J_C=1\ \mu\text{A}/\mu\text{m}^2}$ follow the same trends as in the forward mode for the same reason – namely the variation in the inverse-mode J_{B0} at the V_{BE} for which $J_C = 1\ \mu\text{A}/\mu\text{m}^2$. In all technology platforms, the inverse-mode $\triangle J_B\big|_{V_{BE}=0.6\text{ V}}$ and $\triangle J_B\big|_{J_C=1\ \mu\text{A}/\mu\text{m}^2}$ are both substantially larger than the corresponding forward-mode values, especially at the initial doses in the krad(SiO_2) range. As the cumulative dose approaches 10 Mrad(SiO_2), the forward- and inverse-mode $\triangle J_B\big|_{V_{BE}=0.6\text{ V}}$ and $\triangle J_B\big|_{J_C=1\ \mu\text{A}/\mu\text{m}^2}$ are much closer together. For 3rd-generation HBTs at the final cumulative fluence, the

inverse-mode $\triangle J_B\big|_{V_{BE}=0.6\ \mathrm{V}}$ and $\triangle J_B\big|_{J_C=1\ \mu\mathrm{A}/\mu\mathrm{m}^2}$ are actually larger than the corresponding forward-mode values. It should also be noted that for 1st-generation HBTs, the inverse-mode $\triangle J_B\big|_{V_{BE}=0.6\ \mathrm{V}}$ and $\triangle J_B\big|_{J_C=1\ \mu\mathrm{A}/\mu\mathrm{m}^2}$ are substantially larger than the corresponding (same technology platform) forward-mode $\triangle J_B\big|_{V_{BE}=0.6\ \mathrm{V}}$ and $\triangle J_B\big|_{J_C=1\ \mu\mathrm{A}/\mu\mathrm{m}^2}$ and also larger than the inverse-mode $\triangle J_B\big|_{V_{BE}=0.6\ \mathrm{V}}$ and $\triangle J_B\big|_{J_C=1\ \mu\mathrm{A}/\mu\mathrm{m}^2}$ of all other technology platforms.

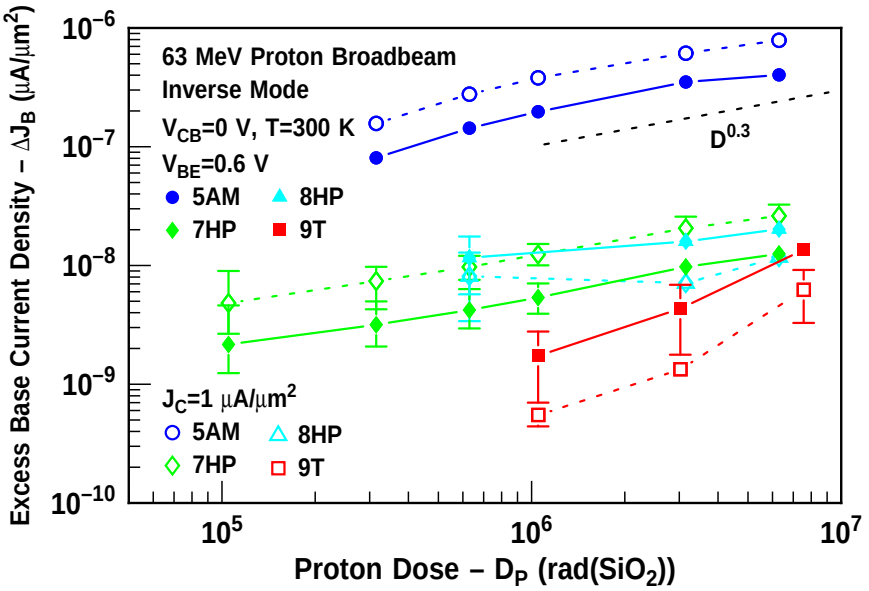

Figure 25: Inverse-mode $\triangle J_B\big|_{V_{BE}=0.6\ \mathrm{V}}$ and $\triangle J_B\big|_{J_C=1\ \mu\mathrm{A}/\mu\mathrm{m}^2}$ vs. 63 MeV proton dose for 1st- through 4th-generation HBTs.

These larger values for the inverse-mode response in 1st-generation HBTs are indicative of an STI that has excessive levels of molecular H_2 incorporated into the film during fabrication [274][275]. Clearly, the STI in the 2nd-, 3rd-, and 4th-generation technology platforms were fabricated in a manner that resulted in substantially less molecular H_2. In addition to the SiO_2 fabrication sequence, the increased STI-to-SIC distance in 2nd-generation HBTs translates into an STI Si/SiO_2 interface that is now physically further removed from the BC depletion region, thereby reducing any interaction with interface traps. Although the migration to the raised-extrinsic-base structure has significant implications for the forward-mode $\triangle J_B\big|_{V_{BE}=0.6\ \mathrm{V}}$ and $\triangle J_B\big|_{J_C=1\ \mu\mathrm{A}/\mu\mathrm{m}^2}$, there is no difference in the inverse-mode $\triangle J_B\big|_{V_{BE}=0.6\ \mathrm{V}}$ and $\triangle J_B\big|_{J_C=1\ \mu\mathrm{A}/\mu\mathrm{m}^2}$ resulting from this new structure.

These findings support the analysis in [244], which suggested that the inverse-mode I_B is dominated by the lateral STI-to-SIC distance.

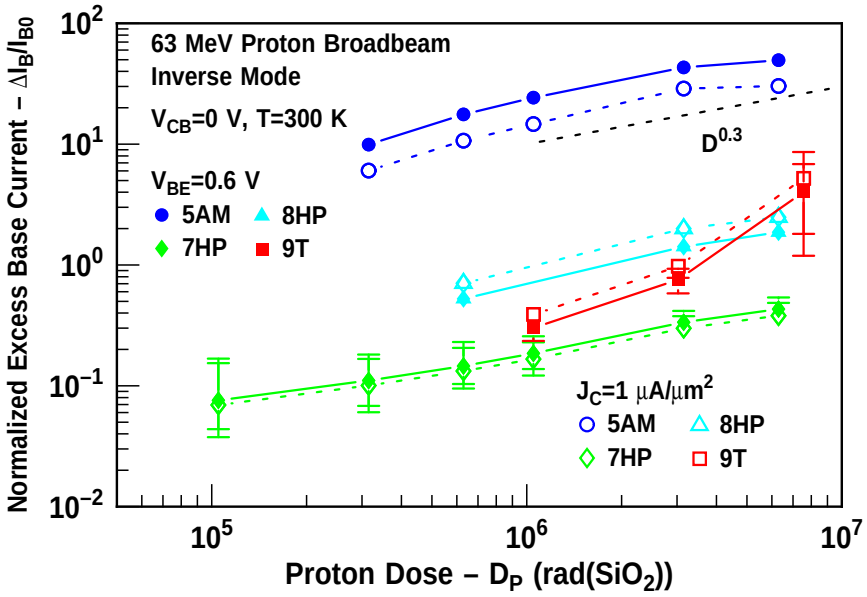

Figure 26: Inverse-mode $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ and $\frac{\triangle I_B}{I_{B0}}\big|_{J_C=1\ \mu\text{A}/\mu\text{m}^2}$ vs. 63 MeV proton dose for 1$^{\text{st}}$- through 4$^{\text{th}}$-generation HBTs.

In the inverse mode, both $\triangle J_B\big|_{V_{BE}=0.6\text{ V}}$ and $\triangle J_B\big|_{J_C=1\ \mu\text{A}/\mu\text{m}^2}$ exhibit a sub-linear ($D^{0.3}$) dependence on dose for all technology platforms. Compared to the linear (D^1) dependence that was observed in the forward mode, the result here is indicative of the onset of saturation effects in ΔI_B. Similar saturation phenomena in $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ have already been demonstrated in Section 3.4 using mixed-mode electrical stress. Saturation phenomena in ΔI_B are a result of the fact that at a certain level of oxide trapped charge, the surface of the p-type base becomes accumulated. This accumulation reduces the recombination rate at the surface of the base ($R_s(y)$) on account of the fact that the peak recombination rate at the surface ($R_{s,pk}$) has shifted below the Si/SiO$_2$ interface [276]. $R_s(y)$ can be written as [276]

$$R_s(y) = \frac{n_i v_{surf} \exp\left(\frac{qV_{BE}}{2k_BT}\right)}{2\cosh\left(\frac{q}{k_BT}\left(\psi_s(y) - \frac{V_{BE}}{k_BT}\right)\right)}, \tag{85}$$

where v_{surf} is the surface recombination velocity and $\psi_s(y)$ is the position-dependent surface

potential. $R_{s,pk}$ can be written as [276]

$$R_{s,pk} = \frac{1}{2} n_i v_{surf} \exp\left(\frac{qV_{BE}}{2k_B T}\right), \tag{86}$$

where all the parameters are the same as defined in (85).

Although the forward- and inverse-mode I_C for 3$^{\text{rd}}$-generation HBTs overlay, the inverse-mode I_B is substantially higher than the forward-mode I_B, as shown in Figure 27. This increase in the inverse-mode I_B is observed for all technology generations and is attributed to the fact that the magnitude of the inverse-mode I_B is dominated by the STI-to-SIC distance, whereas the magnitude of the inverse-mode I_C, forward-mode I_C, and forward-mode I_B are all determined by A_E [244]. Since the inverse-mode I_{B0} is larger than the forward-mode I_{B0}, it follows that the inverse-mode $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ and $\frac{\triangle I_B}{I_{B0}}\big|_{J_C=1\ \mu\text{A}/\mu\text{m}^2}$ are both lower than the forward-mode $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ and $\frac{\triangle I_B}{I_{B0}}\big|_{J_C=1\ \mu\text{A}/\mu\text{m}^2}$ for 2$^{\text{nd}}$-,3$^{\text{rd}}$-, and 4$^{\text{th}}$-generation HBTs. The above analysis shows that there is significant variation in the *dc*-response of SiGe HBTs to medium-energy proton irradiation. Protons are charged particles and induce both atomic displacement and ionization in the transistor. As a result, both the transistor structure, especially the location of the BE spacer and STI, and the doping profiles influence the observed response.

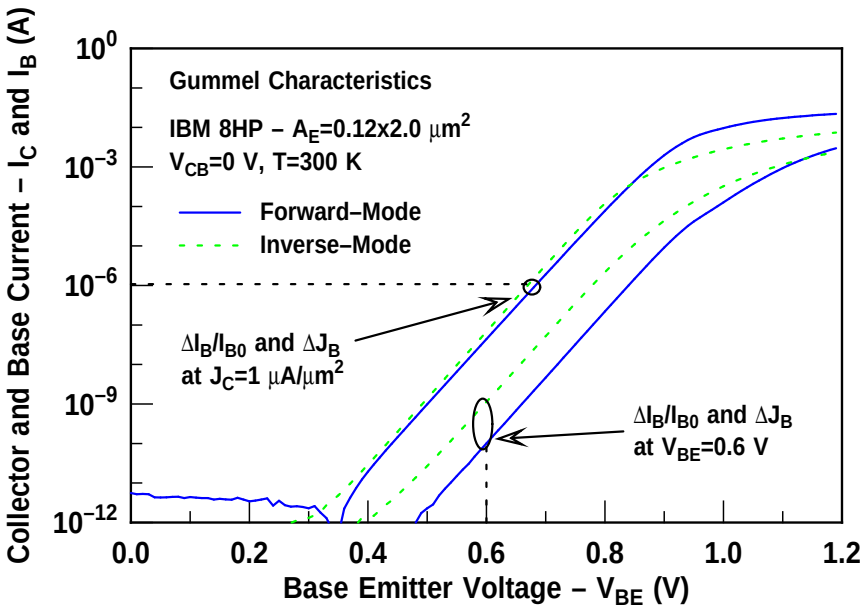

Figure 27: Forward- and inverse-mode Gummel characteristics of 3$^{\text{rd}}$-generation HBTs.

3.5.2 *ac* Performance Degradation

The transistor S-parameters of a 4$^{\text{th}}$-generation HBT were characterized to 45 GHz over a range of bias currents at fixed-V_{CB}. Standard "open-short" structures were used to de-embed the S-parameters and calculate the small-signal current gain (h_{21}) and Mason's Unilateral Gain (U). h_{21} can be written as [6]

$$h_{21} = \frac{i_c}{i_b}\Big|_{v_c=0} = \frac{g_m}{g_{be} + j\omega\left(C_{be} + C_{bc}\right)} = \frac{\beta}{1 + \frac{j\omega(C_{be}+C_{bc})}{g_{be}}}, \tag{87}$$

where i_c is the small-signal collector current, i_b is the small-signal base current, and v_c is the small-signal collector voltage. U can be expressed as [277]

$$U = \frac{|Y_{21} - Y_{12}|^2}{4\left(G_{11}G_{22} - G_{12}G_{21}\right)}, \tag{88}$$

where Y_{ij} are the original short-circuit *Y-parameters* and G_{ij} is the real part of Y_{ij}.

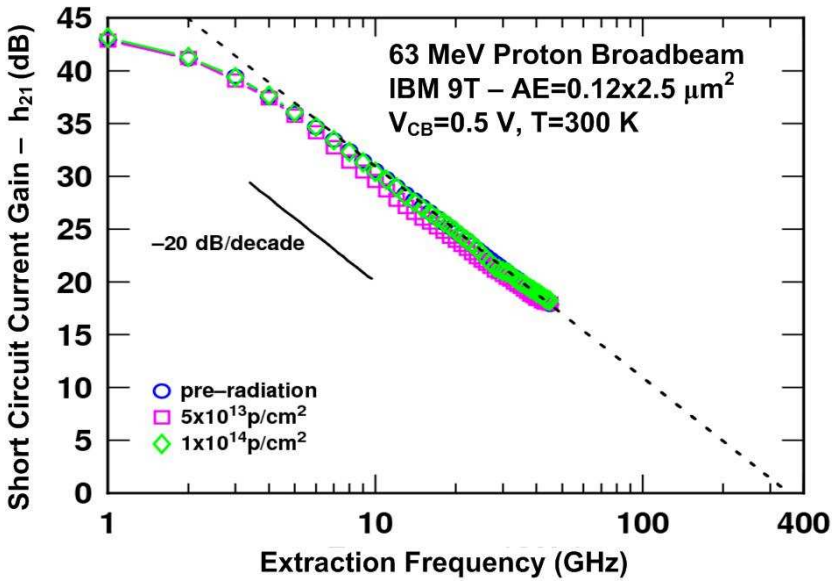

Figure 28: Pre- and post-irradiation h_{21} vs. frequency for 4$^{\text{th}}$-generation HBTs irradiated with 63 MeV protons to a cumulative fluence of 1×10^{14} p/cm^2.

The pre- and post-irradiation h_{21} of a 4$^{\text{th}}$-generation HBT with an A_E of $0.12\times2.5\mu\text{m}^2$ are plotted as a function of extraction frequency in Figure 28. Using a -20 dB/decade slope, the frequency at which h_{21} becomes unity is equivalent to the transistor f_T. Both the pre- and post-irradiation h_{21} are remarkably robust up to a proton fluence of 1.4×10^{14}

p/cm^2. f_{max} is taken as the frequency at which the maximum operating power gain ($G_{p,max}$) becomes unity.

The pre- and post-irradiation f_T and f_{max} are plotted as a function of J_C for 1st- through 4th-generation HBTs in Figures 29 and 30, respectively. As illustrated in Figure 29, the vertical and lateral scaling applied to SiGe HBTs yield higher f_T, occurring at larger J_C values. From a circuit design perspective, significant reductions in power consumption at constant frequency may be obtained by operating a highly scaled HBT at smaller values of J_C.

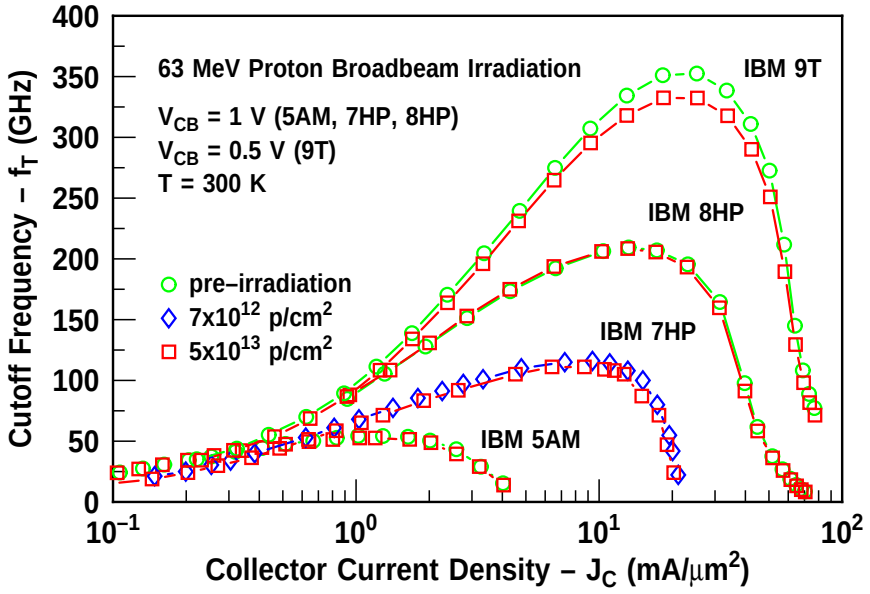

Figure 29: Pre- and post-irradiation f_T vs. J_C for 1st- through 4th-generation HBTs irradiated with 63 MeV protons to a cumulative fluence of 5×10^{13} p/cm^2.

Vertical profile scaling, as applied to SiGe HBTs, is achieved by increasing N_{DC} and N_{AB} while reducing W_B. The transistor-level performance enhancements that are realized by vertical profile scaling include reductions in the base, emitter, and collector transit times (τ_b, τ_e, and τ_c). Unfortunately, these reductions come at the cost of a larger base-collector capacitance (C_{bc}), a larger base resistance (r_b), and a smaller BV_{CEO}. Lateral profile scaling is realized by adjusting the emitter width (W_E) and the STI-to-SIC distance, resulting in reductions in r_b, C_{bc}, and C_{be} (base-emitter overlay capacitance). These capacitance reductions come at the cost of an increased emitter and collector resistance (r_e and r_c,

respectively). At low injection, f_T can be written as [6]

$$f_T = \frac{1}{2\pi\tau_{ec}} = \frac{1}{2\pi}\left[\frac{k_B T}{qI_C}\left(C_{te} + C_{tc}\right) + \tau_b + \tau_e + \frac{W_{CB}}{2v_{sat}} + r_c C_{tc}\right]^{-1}, \tag{89}$$

where τ_{ec} is the emitter-to-collector transit time, C_{te} and C_{tc} are the BE and BC depletion capacitances, W_{BC} is the width of the BC depletion region, and v_{sat} is the carrier saturation velocity. C_{te} is equal to C_{be}, and C_{te} is related to C_{be} by [6]

$$C_{be} = g_m \tau_f + C_{te}, \tag{90}$$

where g_m is the intrinsic transconductance, which can be written as

$$g_m = \frac{kT}{qI_C} = \frac{\partial I_C}{\partial V_{BE}}. \tag{91}$$

At circuit-relevant bias, f_T may also be expressed as [6]

$$f_T = \frac{g_m}{2\pi\left(C_{be} + C_{bc}\right)}. \tag{92}$$

If the relevant substitutions are made for g_m, C_{be}, and C_{bc} in the reciprocal of (92), then f_T can be written as [6]

$$\frac{1}{2\pi f_T} = \tau_f + \frac{k_B T C_t}{qJ_C A_E}, \tag{93}$$

where τ_f is the forward transit time, which dominates at low injection, and $\frac{k_B T C_t}{qJ_C A_E}$ dominates at high injection. The sudden decrease in f_T as J_C is increased past 10 μA/μm^2 occurs as a result of high-injection effects such as the Kirk Effect [278]. Finally, f_{max} can be written in terms of f_T, C_{bc}, and r_b as [6]

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{bc} r_b}}. \tag{94}$$

The 4$^{\text{th}}$-generation HBTs described here feature a collector doping profile that is optimized for enhanced f_T and reduced BV_{CEO}. Although an increased N_{DC} delays the onset of high-injection effects and enables higher f_T, it also increases C_{bc} and $M - 1$. An increase in C_{bc} results in a reduction in f_{max} [6]. Careful profile optimization can also be used to simultaneously improve both f_T and BV_{CEO} as demonstrated in [279][280]. As shown in Figures 29 and 30, there is no proton-induced degradation in either the f_T or f_{max} in the 1$^{\text{st}}$- through 4$^{\text{th}}$-generation HBTs.

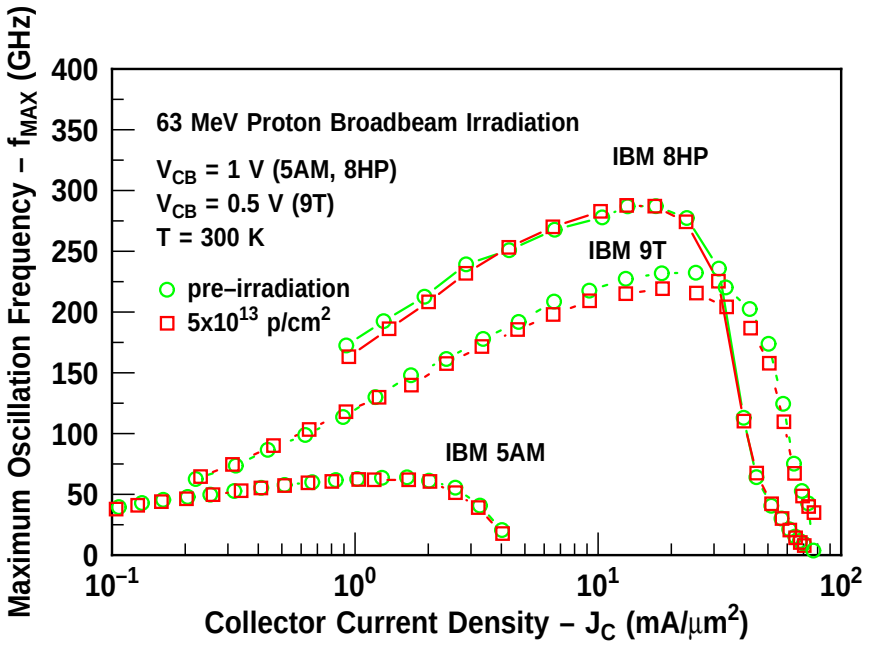

Figure 30: Pre- and post-irradiation f_{max} vs. J_C for 1st- through 4th-generation HBTs irradiated with 63 MeV protons to a cumulative fluence of 5×10^{13} p/cm^2.

In Figure 31, the pre- and post-irradiation r_b are plotted as a function of J_C for 4th-generation HBTs, and in Figure 32, τ_{EF} is plotted as a function of proton fluence for 2nd-, 3rd-, and 4th-generation HBTs.

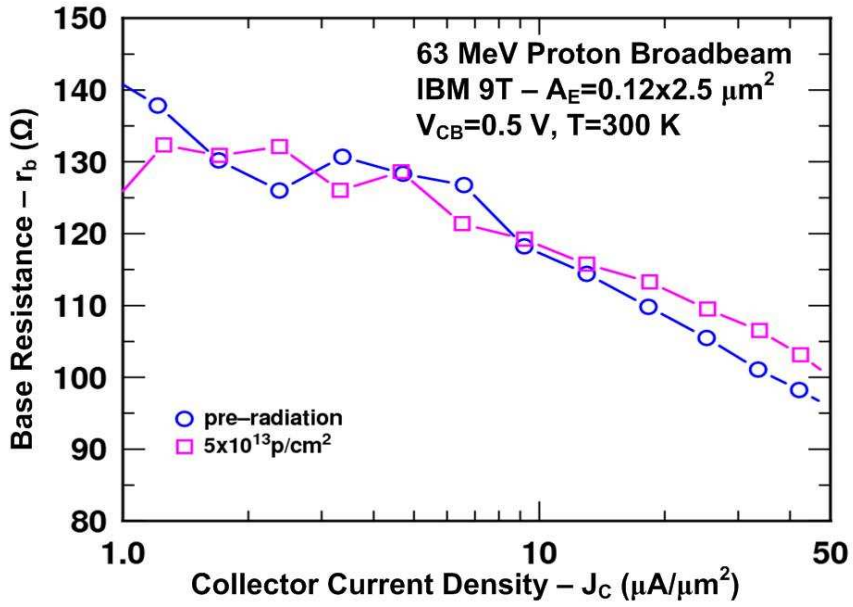

Figure 31: Pre- and post-irradiation r_b vs. J_C for 4th-generation HBTs irradiated with 63 MeV protons to a cumulative fluence of 5×10^{13} p/cm^2.

At a proton fluence of 5×10^{13} p/cm^2, there is no significant change in r_b for J_C values near peak f_T, which is consistent with the lack of degradation in the post-irradiation f_T and f_{max} observed in Figures 29 and 30, respectively. At lower J_C values, there is significant fluctuation in both the pre- and post-irradiation r_b. These fluctuations can be attributed to the fact that the small-signal parameter extraction in this bias regime is less accurate because of the smaller dynamic range of the VNA. Lateral and vertical scaling enable a 69% reduction in τ_{EF}, and as shown in Figure 32, τ_{EF} is independent of proton fluence, which suggests that at this proton energy the displacement-damage component is too low to induce dopant deactivation (reduced r_b) or to increase transit times as was postulated in [281].

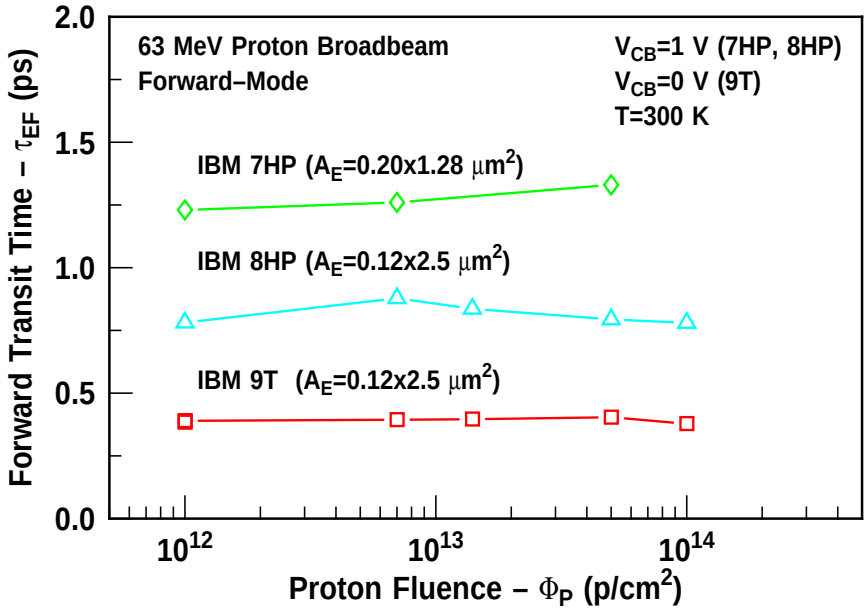

Figure 32: τ_{EC} vs. 63 MeV proton fluence for 2nd- through 4th-generation HBTs.

3.6 Conclusion

The proton tolerance of 1st- through 4th-generation SiGe HBTs has been investigated using 63 MeV protons. Protons are known to cause both atomic displacement and ionization in microelectronic devices and typically represent the "worst case" in degradation for many electronic components. The SiGe HBTs examined in this chapter are remarkably

tolerant to up to 6 Mrad(SiO_2) of 63 MeV protons. This tolerance has been validated using measurements of the *dc*- and *ac*-performance characteristics, low-frequency noise, neutral base recombination, avalanche multiplication, mixed-mode stress, and 2-D TCAD simulations. This multi-Mrad(SiO_2) tolerance is well above the 50 to 300 krad(SiO_2) range that is typical for most space-based electronic components. To be sure, the degree of immunity to proton irradiation is a function of the transistor bias, the location of all Si/SiO_2 interfaces relative to the BE- and BC-depletion regions, and the level of molecular H_2 incorporated into the BE spacer and STI.

CHAPTER 4

HARDNESS ASSURANCE TESTING

4.1 Introduction

In the previous chapter, the radiation-induced performance degradation caused by atomic displacement and ionization in the 1st- through 4th-generation SiGe HBTs was investigated using 63 MeV protons. That investigation is now expanded to include the nuances of the radiation environment on the degradation observed in 1st- and 3rd-generation HBTs. Significant differences in the response of the BE spacer and STI Si/SiO_2 interfaces to ionizing radiation from different sources have been shown to exist for 3rd-generation SiGe HBTs [8]. In that study, 1.2 MeV ^{60}Co gamma irradiation was found to generate increased degradation in the inverse mode, and 63 MeV proton irradiation was found to generate increased degradation in the forward mode. In the literature, there have been several experiments demonstrating large differences in the response of surface and buried oxides to various radiation sources. In SOI MOSFETs, back-gate threshold voltage shifts (ΔV_{TH}) are larger for 1.2 MeV ^{60}Co gamma irradiation than for low-energy x-ray irradiation. This observation was attributed to an increase in charge yield at low electric fields in the buried oxides for gamma irradiation [282][283]. Findings such as these are important since they contribute to the growing body of literature stressing the importance of accurate hardness assurance testing methods for space-based electronic components.

The primary objective of hardness assurance testing is to find the most cost effective irradiation sequence to ensure component qualification for the intended radiation environment. This task becomes increasingly complicated as components become more complex with an increased number of failure modes. In this chapter, an introduction to hardness assurance testing considerations for 1st- and 3rd-generation HBTs is presented by investigating the effect of variations in the radiation source, dose rate, and particle energy relevant to space-based electronic components and high-energy-physics particle detectors.

The impact of the variations in these parameters on transistor performance is considered using the normalized excess base current $\left(\frac{\triangle I_B}{I_{B0}}\right)$, base-current ideality factor (n_{I_B}), proton and neutron displacement damage factors (K_p and K_n), transconductance (g_m), and collector resistance (r_c) as the figures of merit. The results indicate that changes in the radiation environment have profound effects on the post-irradiation performance of these HBTs. Although performance degradation can be correlated to the energy-dependent ionizing LET and NIEL of the radiation source, the doping profile, layer coverage, metal wiring, and oxide fabrication sequence induce secondary effects that are not captured by traditional theories.

4.2 Hardness Assurance Testing for Space-Based Electronics

4.2.1 Experiment Details

In-situ irradiation was performed on 3$^{\text{rd}}$-generation SiGe HBTs, with an A_E of 0.12×1, 0.12×2, 0.12×4, and 0.12×8 μm^2, packaged into 28-pin DIPs using the procedure described in Section 3.2. 63 MeV proton irradiation was performed at the CNL facility [203][204], 1.2 MeV ^{60}Co gamma irradiation was performed at the NASA GSFC facility [207], and 10 keV x-ray irradiation was performed at Vanderbilt University [215][216]. Each radiation facility is described in detail in Section 2.3. By convention, all dose values are normalized to rad(SiO_2). In a 10 keV x-ray environment, 1 rad(Si) is equivalent to 1.8×rad(SiO_2), but in a 63 MeV proton or 1.2 MeV ^{60}Co gamma environment, the equivalent dose in Si and SiO_2 differ by less than 5%.

4.2.2 Radiation-Induced Excess Base Current

In this section, the variation in the forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$ is used to compare damage to the BE spacer and STI resulting from proton, gamma, and x-ray irradiation. Going forward, the "V_{BE}=0.6 V" subscript will be dropped from $\frac{\triangle I_B}{I_{B0}}\big|_{V_{BE}=0.6\text{ V}}$. The forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}$ are compared for 63 MeV proton, 1.2 MeV ^{60}Co gamma, and 10 keV x-ray irradiation of 1$^{\text{st}}$- and 3$^{\text{st}}$-generation HBTs in Figures 33 and 34, respectively. The forward-mode $\frac{\triangle I_B}{I_{B0}}$ values are indicated using solid lines and closed symbols, while the inverse-mode $\frac{\triangle I_B}{I_{B0}}$ values are indicated using dashed lines and open symbols.

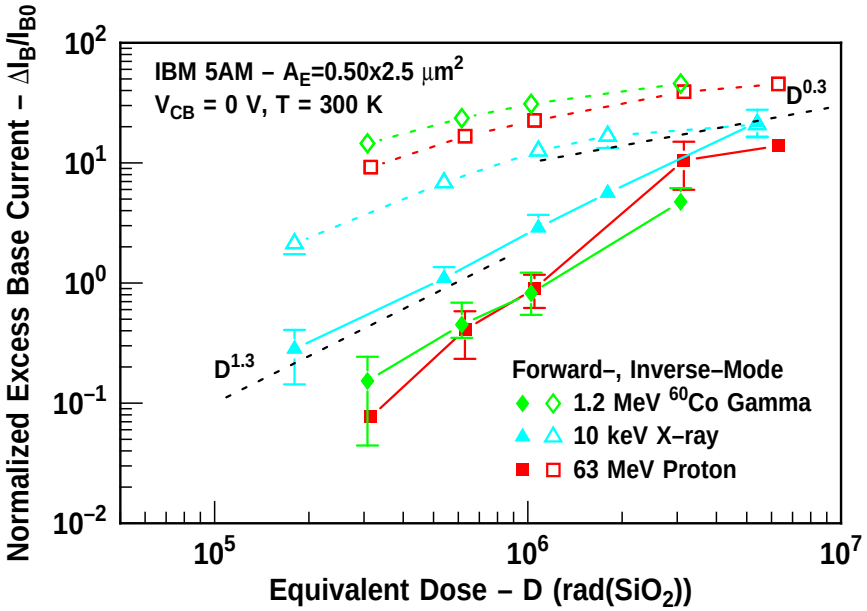

Figure 33: Forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}$ vs. equivalent dose for 1st-generation HBTs irradiated with 1.2 MeV ^{60}Co gamma rays, 10 keV x-rays, and 63 MeV protons.

In Figures 35 and 36, the forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}$ are re-plotted on a linear scale to emphasize the enhanced degradation in the inverse mode.

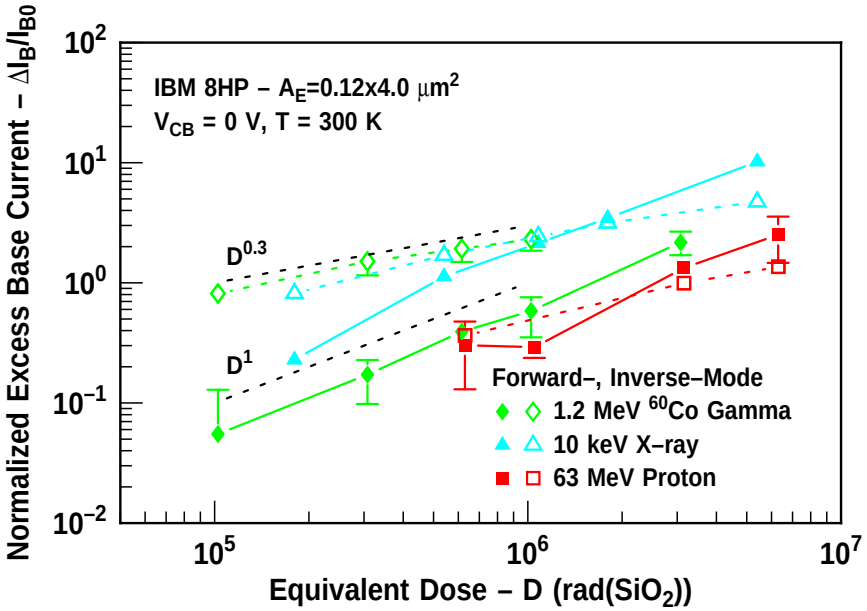

Figure 34: Forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}$ vs. equivalent dose for 3rd-generation HBTs irradiated with 1.2 MeV ^{60}Co gamma rays, 10 keV x-rays, and 63 MeV protons.

Each data point represents the average $\frac{\triangle I_B}{I_{B0}}$ for a sample size of between two to four transistors, and the error bars correspond to the maximum and minimum values of $\frac{\triangle I_B}{I_{B0}}$ in each sample. If there are no error bars, then the sample variation is very small. The dose rates corresponding to the proton, gamma, and x-ray sources are 1 krad(SiO_2)/s, 30 rad(SiO_2)/s, and 540 rad(SiO_2)/s, respectively.

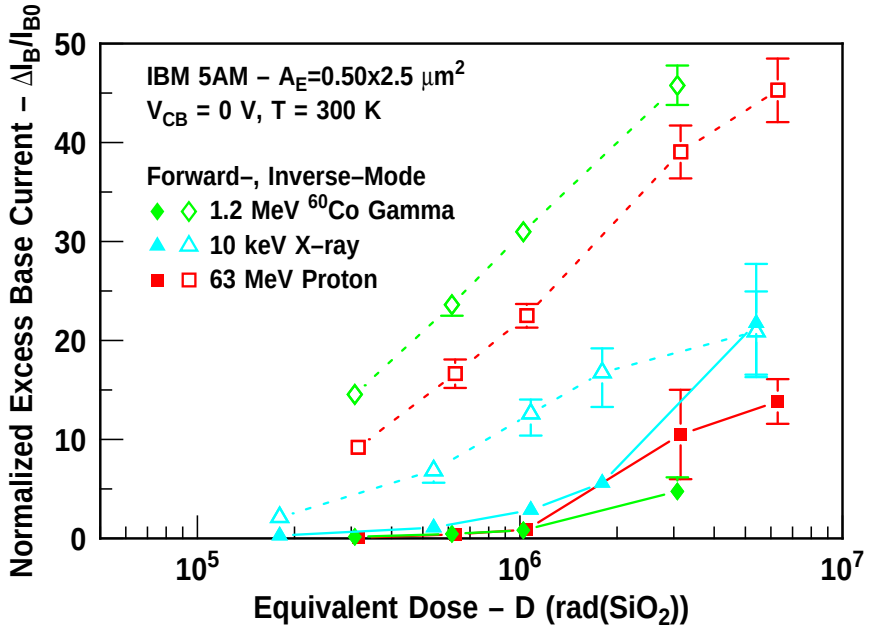

Figure 35: Figure 33 re-plotted with $\frac{\triangle I_B}{I_{B0}}$ on a linear scale to emphasize increased degradation in the inverse mode.

The post-irradiation response of 1st-generation HBTs, illustrated in Figure 33, is considered first. Regardless of the radiation source, the forward-mode $\frac{\triangle I_B}{I_{B0}}$ exhibits a super-linear ($D^{1.3}$) dose dependence and is substantially smaller than the inverse-mode $\frac{\triangle I_B}{I_{B0}}$, which exhibits a sub-linear ($D^{0.3}$) dose dependence. In the forward mode, the proton- and gamma-induced $\frac{\triangle I_B}{I_{B0}}$ are well-matched up to 3 Mrad(SiO_2) and, at doses below 3 Mrad(SiO_2), are substantially smaller than the x-ray-induced $\frac{\triangle I_B}{I_{B0}}$. Conversely, in the inverse mode, the gamma-induced $\frac{\triangle I_B}{I_{B0}}$ is slightly larger than the proton-induced $\frac{\triangle I_B}{I_{B0}}$ and substantially larger than the x-ray-induced $\frac{\triangle I_B}{I_{B0}}$.

The post-irradiation response of 3rd-generation HBTs, illustrated in Figure 34, is now considered. A comparison of the y-axes of Figures 35 and 36 illustrates the improvement in the radiation tolerance of 3rd-generation HBTs for all radiation sources. Several observations

can be made regarding the radiation response of 1st- and 3rd-generation HBTs. First, as was observed for 1st-generation HBTs, the forward-mode $\frac{\triangle I_B}{I_{B0}}$ exhibits a linear (D^1) dose dependence and the inverse-mode $\frac{\triangle I_B}{I_{B0}}$ exhibits a sub-linear ($D^{0.3}$) dose dependence. Next, in the forward mode, the x-ray-induced $\frac{\triangle I_B}{I_{B0}}$ is again substantially larger than both the proton- and gamma-induced $\frac{\triangle I_B}{I_{B0}}$. However, in contrast to the 1st-generation response, the gamma-induced $\frac{\triangle I_B}{I_{B0}}$ is slightly larger than the proton-induced $\frac{\triangle I_B}{I_{B0}}$. Third, in the inverse mode, the gamma- and x-ray-induced $\frac{\triangle I_B}{I_{B0}}$ are now both substantially larger than the proton-induced $\frac{\triangle I_B}{I_{B0}}$. This last result is the opposite of what was observed in the 1st-generation response, which had gamma- and proton-induced $\frac{\triangle I_B}{I_{B0}}$ values that were both larger than the x-ray-induced $\frac{\triangle I_B}{I_{B0}}$.

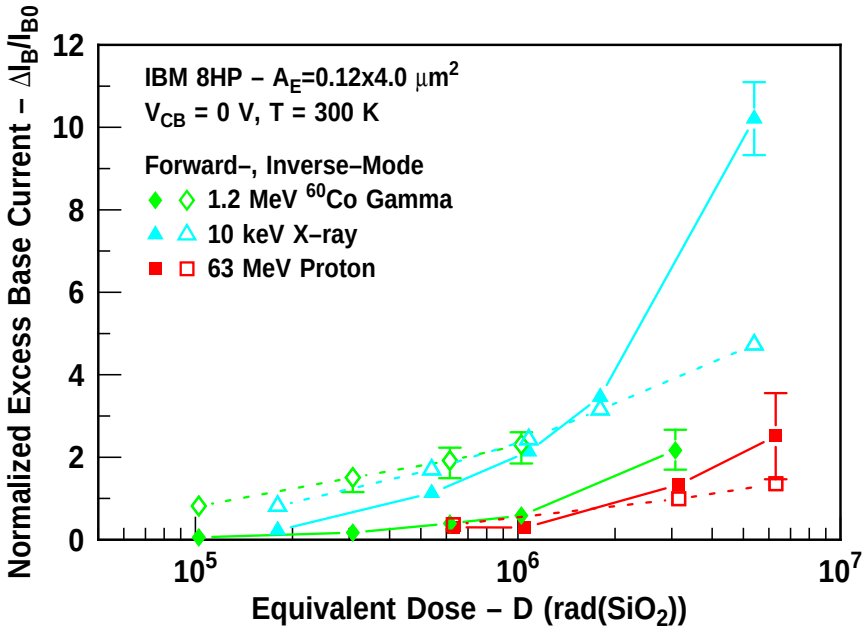

Figure 36: Figure 34 re-plotted with $\frac{\triangle I_B}{I_{B0}}$ on a linear scale to emphasize increased degradation in the inverse mode.

The variation in the forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}$ as a function of radiation source can be partially explained by considering relationship between particle LET and energy, as illustrated in Figure 37 [268]. Radiation-induced degradation from x-ray and gamma sources occurs via the creation of secondary electrons from photon interaction with either Si or SiO_2. These electrons go on to interact with the bulk SiO_2, which results in the creation of oxide trapped charge and Si/SiO_2 interface traps. Therefore, the "particle LET" for a

10 keV x-ray photon or a 1.2 MeV ^{60}Co gamma-ray photon may be derived from their secondary electrons, as indicated in Figure 37. Carrier recombination in the bulk SiO_2 for particle LETs above 100 MeV·cm^2/mg is described using the columnar model, as described in Section 2.2 and [125][127], while for LETs below 100 MeV·cm^2/mg, the geminate model, also described in Section 2.2, is more appropriate [126].

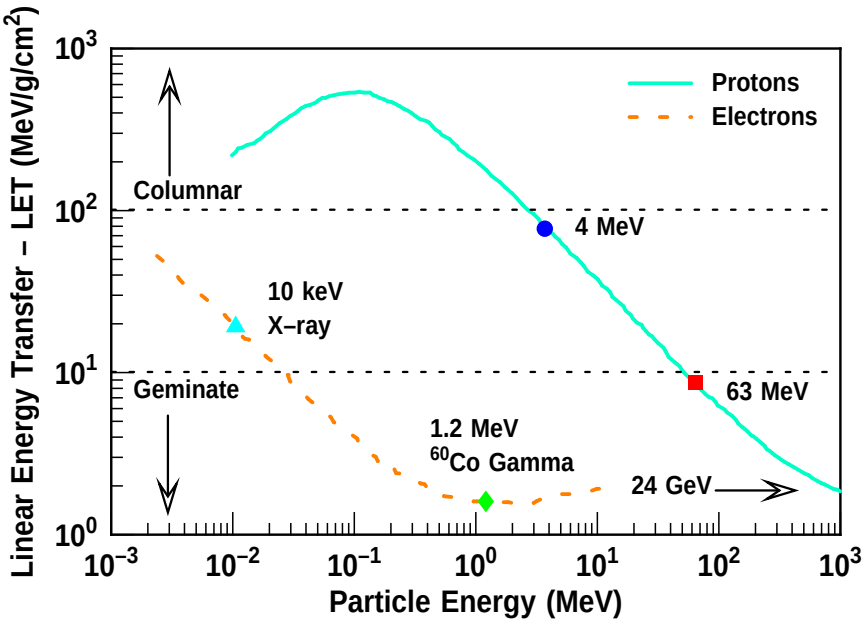

Figure 37: Electron and proton LET vs. particle energy [284].

Of the three radiation sources considered thus far, the LET of the secondary electrons generated by 10 keV x-rays, which is approximately 25 MeV·cm^2/g, is closest to the lower threshold of the columnar model. Conversely, the LET of the secondary electrons generated by 1.2 MeV ^{60}Co gamma rays, which is approximately 2 MeV·cm^2/g, is within the regime of the geminate model. Finally, the LET of 63 MeV protons, which is approximately 8 MeV·cm^2/g, falls in between that of 10 keV x-rays and 1.2 MeV ^{60}Co gamma rays and is just below the upper threshold of the geminate model. As discussed in Section 2.2, the probability of radiation-induced carrier recombination in bulk SiO_2 is lower in the geminate regime since the excess e-h pairs are generated with greater spatial separation. Therefore, the charge yield for particle LETs in the geminate regime is larger than in the columnar regime. An increased charge yield translates into an increase in both the oxide trapped

charge and Si/SiO_2 interface trap density.

If charge yield in the bulk SiO_2 dominates the post-irradiation response, then one would expect 1.2 MeV ^{60}Co gamma-rays to be the most damaging source, followed by 63 MeV protons, and then 10 keV x-rays. This trend is observed when the proton- and gamma-induced $\frac{\triangle I_B}{I_{B0}}$ are compared, but not when the comparison is extended to include x-rays. The particle LET trends described in Figure 37 correlate well with the inverse-mode $\frac{\triangle I_B}{I_{B0}}$ of 1^{st}-generation HBTs shown in Figure 35 but they only partially explain the inverse-mode $\frac{\triangle I_B}{I_{B0}}$ of 3^{rd}-generation HBTs shown in Figure 36. In 3^{rd}-generation HBTs, the x-ray-induced $\frac{\triangle I_B}{I_{B0}}$ is comparable to the gamma-induced $\frac{\triangle I_B}{I_{B0}}$ and larger than the proton-induced $\frac{\triangle I_B}{I_{B0}}$.

This enhancement in the x-ray-induced $\frac{\triangle I_B}{I_{B0}}$ occurs in both the forward and inverse mode and may be attributed to *dose enhancement* effects, which are known to occur in a low-energy x-ray environment. Dose enhancement occurs when low-energy x-ray photons, with $E_{ph} \lll 1$ MeV, interact with high-Z materials and create more e-h pairs than if those high-Z materials were not present. The increase in the number of e-h pairs that are created is the result of photon interaction with high-Z materials via the photoelectric effect, which has a pair creation rate that is proportional to Z^4 [285][286]. These dose-enhancement-generated carriers then interact with both the Si and SiO_2 regions in the transistor, thereby depositing a larger dose into the transistor than at the surface of the die. Conversely, high-energy photons, with $E_{ph} \ggg 1$ MeV, interact with high-Z materials via Compton scattering, which has a pair creation rate that is independent of Z and thus not affected by the presence or absence of high-Z materials [287].

There are several factors which suggest that dose enhancement may be a valid concern in these HBTs when irradiated with 10 keV x-rays. First, the photon energy is low enough for the photoelectric effect to dominate e-h pair generation. Second, the transistor contacts, which are made of high-Z copper- and tungsten-metal studs, are located very close to the sensitive Si and SiO_2 regions, as illustrated in Figures 2 and 3. In both technology platforms, the BE spacer is located considerably closer to these studs than the STI. This variation is consistent with the fact that the enhanced x-ray response is more pronounced in the forward mode, as illustrated in Figures 33 and 34. Third, in 3^{rd}-generation HBTs, the combination

of the raised-extrinsic-base structure and the utilization of vertical profile scaling means that the BE junction, BC junction, and STI are all now physically closer to the high-Z studs. Finally, the BEOL metalization stack in the 3rd-generation platform consists of seven metal layers, while the BEOL stack in the 1st-generation platform is a five-layer stack. Therefore, the density of high-Z materials in the 3rd-generation platform is larger, and dose enhancement effects for 10 keV x-rays are more likely to occur in this platform. Dose enhancement effects have also been verified in older CMOS technology platforms as well as in GEANT-4 simulations for SRAMs [288]-[292]. Comparisons of the radiation-induced degradation following 10 keV x-ray and 1.2 MeV ^{60}Co gamma irradiation for surface and buried oxides in MOS technologies have also been done in [282]-[284][293][294] and yield results similar to those presented in this section.

4.2.3 Base-Current Ideality Factors

The contributions of surface and subsurface SRH recombination to the radiation-induced ΔI_B can be determined by examining the base-current ideality factor (n_{I_B}). The radiation-induced recombination current in the base varies in proportion to exp $\left(\frac{qV_{BE}}{k_BTn_{I_B}}\right)$, and if n_{I_B} lies between one and two, then surface SRH recombination involving Si/SiO_2 interface traps near the BE depletion region (for the forward mode) or BC depletion region (for the inverse mode) is the dominant physical mechanism [295]. Conversely, if n_{I_B} is equal to two, then recombination is dominated by sub-surface SRH processes in the bulk SiO_2 [296].

The *charge separation* method has been applied in [296] to qualitatively separate the damage mechanisms for different radiation sources. As originally proposed, this approach is based on the analysis of the variation in the slope of ΔI_B ($n_{\Delta I_B}$) as a function of V_{BE}. When plots of ΔI_B vs. V_{BE} for silicon BJTs were examined in [296], two distinct regions were defined. The first was a low-V_{BE} region, for which n_{I_B} lies between one and two, and the second was a high-V_{BE} region, for which n_{I_B} is equal to two. The transition voltage (V_{tr}) between the high- and low-V_{BE} regions was then used to determine the quantity of oxide trapped charge. Unlike the BJTs investigated in [296], n_{I_B} is never greater than two for

these 3rd-generation SiGe HBTs, as illustrated in Figure 38 for 63 MeV proton irradiation to a cumulative dose of 6 Mrad(SiO_2) at a dose rate of 1 krad(SiO_2)/s. This result suggests that surface SRH recombination is the dominant mechanism behind the radiation-induced ΔI_B for these irradiation conditions.

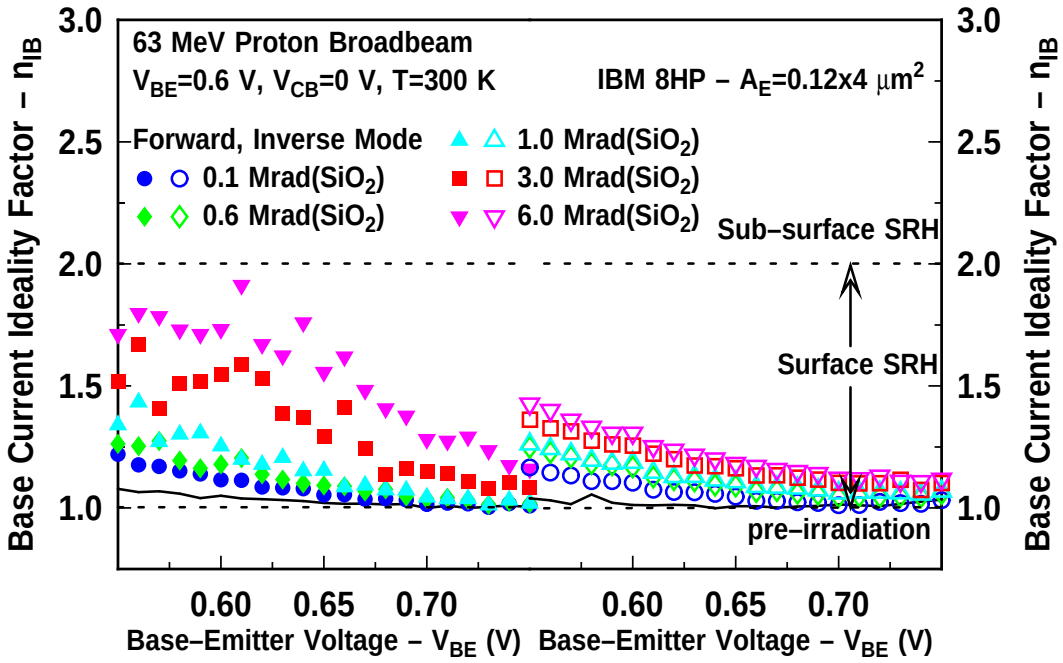

Figure 38: Forward- and inverse-mode $n_{\Delta I_B}$ vs. V_{BE} for 3rd-generation HBTs irradiated with 63 MeV protons to a cumulative dose of 6 Mrad(SiO_2).

The increase in n_{I_B} as a function of dose is caused by an increase in the non-ideal component of the base current (J_{B1} in (63)). In Figures 39 and 40, the forward- and inverse-mode $n_{\Delta I_B}$ are extracted following proton, gamma, and x-ray irradiation of 1st- and 3rd-generation HBTs to 3 Mrad(SiO_2). The dose rate for protons was 1 krad(SiO_2)/s, the dose rate for gammas was 30 rad(SiO_2)/s, and the dose rate for x-rays was 540 rad(SiO_2)/s. Trend lines have been included on these figures to indicate the pre-irradiation n_{I_B} value, which is ideally equal to one, and the regions where surface SRH ($1 \leqslant n_{\Delta I_B} \leqslant 2.0$) and sub-surface SRH ($n_{\Delta I_B} \approx 2.0$) are assumed to dominate.

The post-irradiation base-current ideality factors of 1st-generation HBTs, which are shown in Figure 39, are considered first. In the forward mode, $n_{\Delta I_B}$ varies between 1.75 and 1.90 for all radiation sources, which indicates that surface SRH recombination dominates the

observed post-irradiation ΔI_B. Conversely, in the inverse mode, the proton- and gamma-induced $n_{\Delta I_B}$ vary between 1.50 and 1.90, and the x-ray-induced $n_{\Delta I_B}$ is significantly smaller than both the proton- and gamma-induced $n_{\Delta I_B}$. Furthermore, for all radiation sources, $n_{\Delta I_B}$ fluctuates much less in the inverse mode than in the forward mode.

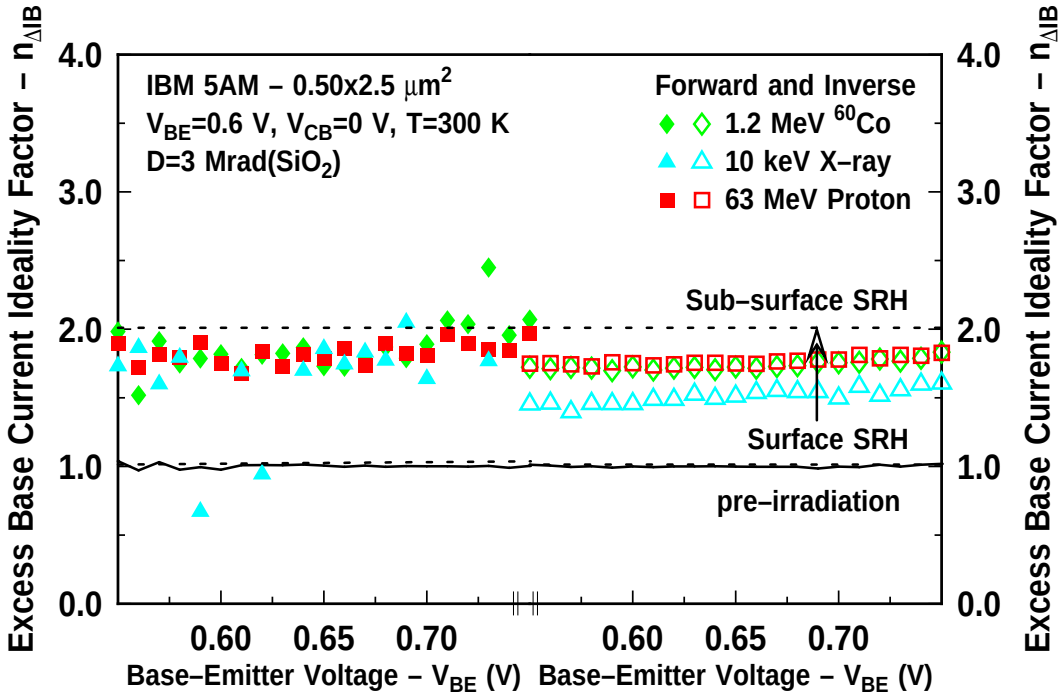

Figure 39: Forward- and inverse-mode $n_{\Delta I_B}$ vs. V_{BE} for 1st-generation HBTs irradiated with 1.2 MeV ^{60}Co gamma rays, 10 keV x-rays, and 63 MeV protons.

Three key differences are observed when the post-irradiation $n_{\Delta I_B}$ (at 3 Mrad(SiO_2)) of 1st-generation HBTs is compared to that of 3rd-generation HBTs. First, the fluctuations in the forward-mode $n_{\Delta I_B}$ of 3rd-generation HBTs ($1.5 \leqslant n_{\Delta I_B} \leqslant 2.5$) are much larger than for 1st-generation HBTs ($1.75 \leqslant n_{\Delta I_B} \leqslant 1.9$). This difference in the range of the forward-mode $n_{\Delta I_B}$ as a function of V_{BE} is indicative of a variation in the thickness and quality of the BE spacer of the two technology platforms. Second, in the forward mode, $n_{\Delta I_B}$ is much greater than two for 3rd-generation HBTs irradiated with protons and x-rays but not for those irradiated with gamma rays. This result indicates that at these cumulative doses, surface SRH recombination dominates the gamma response, while a combination of sub-surface SRH recombination and BE spacer tunneling may be present in the proton and x-ray response. This tunneling component may be attributed to the incorporation of silicided base

contacts, the utilization of the raised-extrinsic-base structure, and the presence of a thinner BE spacer in 3rd-generation HBTs.

It should also be noted that the BE spacer is a complicated SiO_2/Si_3N_4 composite stack [297][298], whereas the STI is deposited using chemical vapor deposition (CVD). Different deposition techniques yield surface and buried oxides with different levels of molecular H_2 incorporated into the film. Finally, in 3rd-generation HBTs, the inverse-mode $n_{\Delta I_B}$ is approximately equal to 1.40 for all radiation sources, which indicates that charge yield in the STI of this platform is less than in the 1st-generation platform. Furthermore, the fact that the x-ray-induced $n_{\Delta I_B}$ is equal to the proton- and gamma-induced $n_{\Delta I_B}$ indicates that x-ray-induced dose enhancement effects in 3rd-generation HBTs do indeed result in greater energy deposition and increased charge yield. These results are consistent with the $\frac{\Delta I_B}{I_{B0}}$ results presented in the previous section.

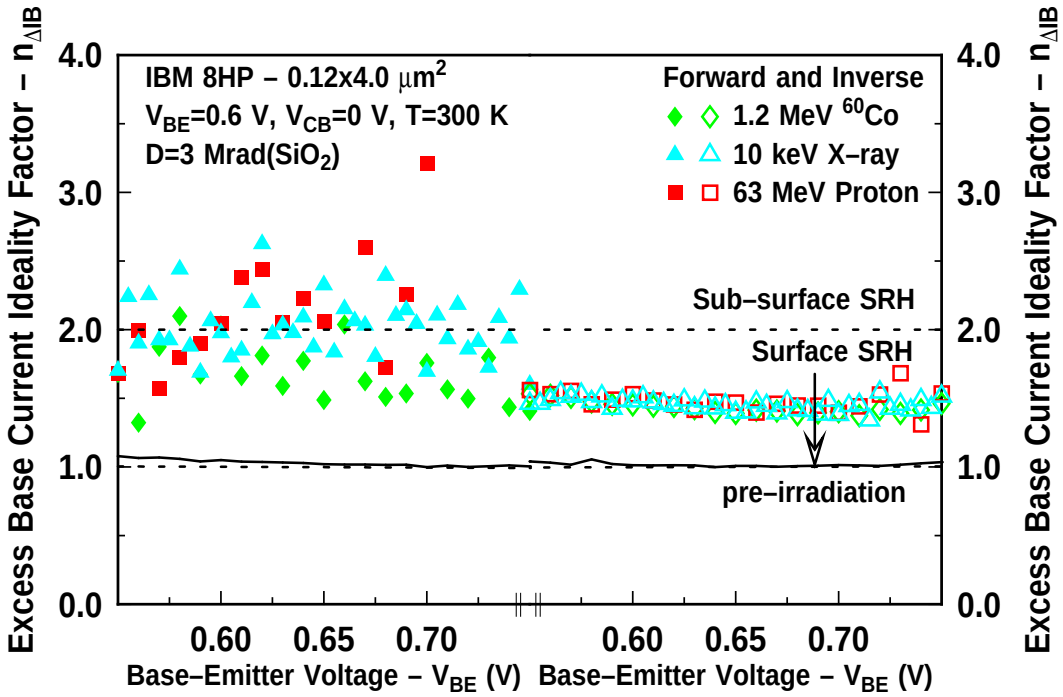

Figure 40: Forward- and inverse-mode $n_{\Delta I_B}$ vs. V_{BE} for 3rd-generation HBTs irradiated with 1.2 MeV ^{60}Co gamma rays, 10 keV x-rays, and 63 MeV protons.

4.2.4 Dose Rate Effects

The investigations into the impact of the radiation source on performance degradation was presented using a different dose rate for each source. To ascertain whether source comparisons at different dose rates are justified, irradiations for each source were repeated at between two to four dose rates, as illustrated in Figure 41 for 3rd-generation SiGe HBTs. Over dose rates ranging from 30 rad(SiO_2)/s to 1 krad(SiO_2)/s, there is a slight reduction in both the forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}$ following 63 MeV proton irradiation. For 10 keV x-ray irradiation, a similar trend is observed as the dose rate is reduced from 54 to 540 rad(SiO_2)/s but with less of a variation in the inverse mode. Conversely, in a 1.2 MeV ^{60}Co gamma environment, there is noticeable decrease in both the forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}$ as the dose rate is reduced from 30 to 0.1 rad(SiO_2)/s. These results suggest that an *Enhanced Low Dose Rate Sensitivity* (ELDRS) effect does indeed exist in these 3rd-generation SiGe HBTs and that it is a function of the radiation source.

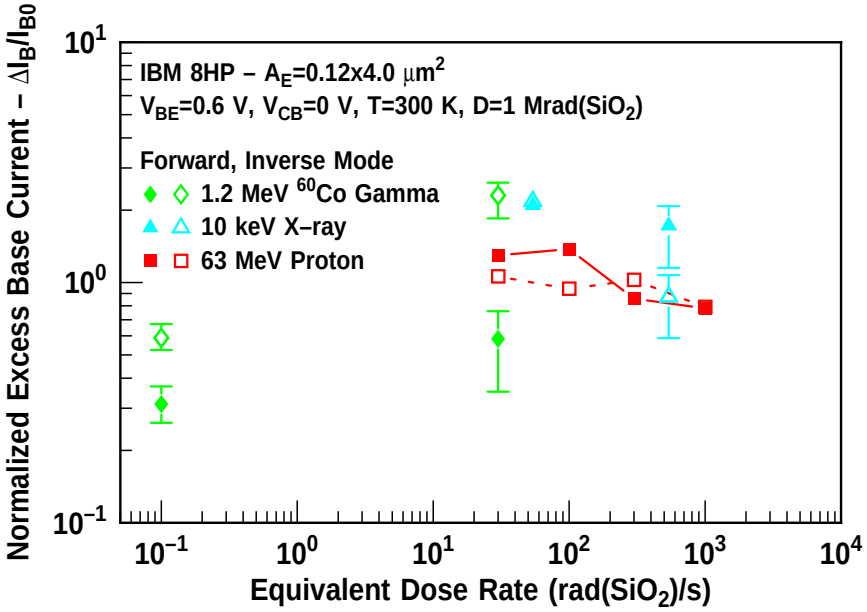

Figure 41: Forward- inverse-mode $\frac{\triangle I_B}{I_{B0}}$ vs. dose rate for 3rd-generation HBTs irradiated with 1.2 MeV ^{60}Co gamma rays, 10 keV x-rays, and 63 MeV protons to a cumulative dose of 1 Mrad(SiO_2).

Ionization-induced ΔI_B in vertical BJTs was found to be a strong function of the dose rate in [276],[299]-[303]. ELDRS is particularly pronounced between dose rates of 0.1 to

10 rad(SiO_2)/s, is less noticeable at extremely high or low dose rates, and is dependent on the technology platform, transistor bias, and oxide quality and thickness. ELDRS in space-based electronic components is of particular concern since although space-relevant dose rates are usually below 0.01 rad(SiO_2)/s, most ground-based irradiation facilities use dose rates greater than 50 rad(SiO_2)/s [161].

The two most popular models describing ELDRS effects in vertical BJTs are now described. In the first model, which is invoked at high dose rates, the rate of trapped charge formation in bulk SiO_2 is assumed to be faster than the transit time for unrecombined holes to be transported to the Si/SiO_2 interface. Depending on the difference in the time required for the creation of oxide trapped charge and the time required hole transport, a dose-rate-dependent space charge region is created in the bulk SiO_2, which eventually retards the transport of additional holes to the interface [304][305]. At low dose rates, this space charge region does not have enough time to grow sufficiently large to effectively retard hole transport. Therefore, ΔI_B is increased as more holes reach the Si/SiO_2 interface. The dose-rate dependence of this effect is dramatically reduced as the dose rate is either reduced or increased beyond the regime in which the effect is observed.

In the second model, the creation of Si/SiO_2 interface traps is based on the reaction between two precursors. The first precursor is generated far from the interface, with a relatively long transport time, and the second precursor is generated very close to the interface, with a significantly shorter transport time [306][307]. This model assumes that the second precursor is available only during irradiation. Therefore, if the irradiation time is longer than the transport time of the first precursor, degradation is enhanced. Several other less-popular ELDRS models have been proposed. In [270], V_{BE} was shown to be extremely influential in the low-energy x-ray response at low dose rates. This conclusion was derived based on observations of transistors biased in the forward mode exhibiting enhanced degradation by a factor of two for npn BJTs and three for pnp BJTs. The interaction of fringing electric fields with the screen oxide was proposed as the physical mechanism driving these experimental observations. In a second study by the same group, the presence of shallow electron traps in the bulk SiO_2 was proposed as the damage mechanism behind the

observed low-dose-rate response of vertical BJTs [308].

4.3 Hardness Assurance Testing for High-Energy-Physics Experiments

Thus far, most of the investigations into the tolerance of SiGe HBTs to atomic displacement and ionization have been done up to a maximum 1.2 MeV ^{60}Co gamma dose of 6 Mrad(SiO_2) [9][309], a maximum 63 MeV proton fluence of 10^{13} p/cm^2 [7][239][310], and a maximum 1 MeV neutron fluence of 10^{15} n/cm^2 [311]. Although these radiation levels are significantly higher than what would be encountered in a typical satellite orbit [16], the detector electronics employed in high-energy-physics experiments, such as the LHC at CERN, are exposed to significantly higher dose and fluence [199]. To be sure, investigations of radiation-induced degradation in particle detectors at high dose and fluence have been performed in [312]-[316]. Furthermore, in [316], 1st-generation SiGe HBTs were exposed to 24 GeV proton irradiation up to a fluence of 10^{16} p/cm^2, and the resultant degradation was found to be less than that of a standard Si BJT. Moreover, the post-irradiation β was still within the range acceptable for use in the ATLAS detector [317].

In this section, the investigations in [316] are expanded by considering the tolerance of 3rd-generation SiGe HBTs to extremely high levels of atomic displacement and ionization. The findings provide a more comprehensive outlook on the suitability of SiGe HBTs for high-energy-physics detector electronics and offer further insight into the underlying physical mechanisms behind the variation in the observed radiation-induced degradation as a function of technology scaling, transistor geometry, and bias.

4.3.1 Experiment Details

1st-generation HBTs with an A_E of 0.5 × 1.0, 0.5 × 2.5, and 0.5 × 20 × 2 μm^2 and 3rd-generation HBTs with an A_E of 0.12 × 1.0, 0.12 × 2.0, 0.12 × 4.0, and 0.12 × 8.0 μm^2 were each packaged separately into custom-made PCBs according to the technology node and radiation source. For the 24 GeV proton and 100 keV neutron sources, the post-irradiation data was collected on a separate PCB for each fluence. Conversely, for the 1.2 MeV ^{60}Co gamma source, the same PCB was used for each intermediate dose step. Proton

and gamma irradiation were performed with all terminals grounded and under forward-active bias (V_{SX}=V_C=V_B=0 V and V_E=-0.8 V), while neutron irradiation was performed with all terminals grounded.

Proton irradiation was performed at CERN facility [205] in collaboration with the RD50 project [318], neutron irradiation was performed at the Ljubljana nuclear reactor using a combination of fast and thermal neutrons in a 1:2 flux ratio [209]-[213], and gamma irradiation was performed at the BNL facility [208]. Each radiation facility has been described in detail in Section 2.3.

4.3.2 Proton Energy Effects

The post-irradiation forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}$ for 1st- and 3rd-generation HBTs are plotted in Figures 42 and 43 after irradiation with protons of energy 4 MeV, 63 MeV, and 24 GeV, and neutrons of energy 1 MeV.

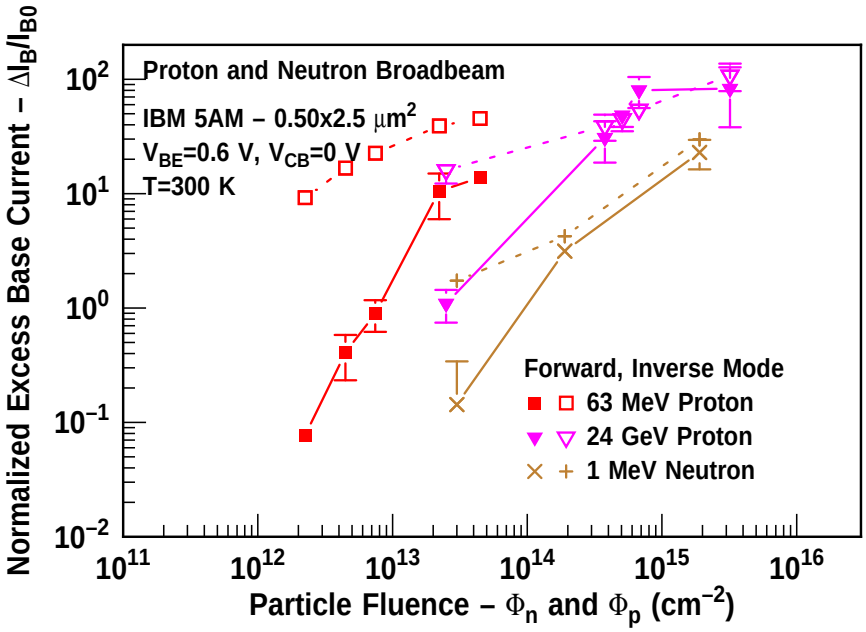

Figure 42: Forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}$ vs. Φ_P and Φ_N for 1st-generation HBTs irradiated with 1 MeV neutrons, 63 MeV protons, and 24 GeV protons.

In these figures, the energy deposited into the transistor is measured using the proton and neutron particle fluence (Φ_n and Φ_p). Each data point represents the average $\frac{\triangle I_B}{I_{B0}}$ for samples of between two to four transistors, and the error bars correspond to the maximum

and minimum values of $\frac{\triangle I_B}{I_{B0}}$ in each sample. If there are no error bars, then the sample variation is very small. Proton and neutron-induced degradation in 1st-generation HBTs, as shown in Figure 42, are considered first. First, for proton irradiation to a moderate fluence of 2.0×10^{13} p/cm^2, $\frac{\triangle I_B}{I_{B0}}$ at 24 GeV is less than $\frac{\triangle I_B}{I_{B0}}$ at 63 MeV. Second, as the fluence is increased to 3.2×10^{15} p/cm^2, $\frac{\triangle I_B}{I_{B0}}$ saturation is observed at 24 GeV, and based on the trends for 63 MeV proton irradiation, saturation at lower proton energies is also expected. Finally, the neutron-induced $\frac{\triangle I_B}{I_{B0}}$ is an order of magnitude lower than the proton-induced $\frac{\triangle I_B}{I_{B0}}$ at both 63 MeV and 24 GeV. The above trends are observed both in the forward and inverse mode. With the addition of 4 MeV protons, the neutron- and proton-induced degradation in 3rd-generation HBTs, as shown in Figure 43, are now considered. The post-irradiation $\frac{\triangle I_B}{I_{B0}}$ values at 63 MeV and 24 GeV are equal and are both significantly smaller than at 4 MeV. This trend is also observed in both the forward and inverse mode. In contrast to the 1st-generation HBT data, the proton- and neutron-induced $\frac{\triangle I_B}{I_{B0}}$ values are very closely matched at the final fluence.

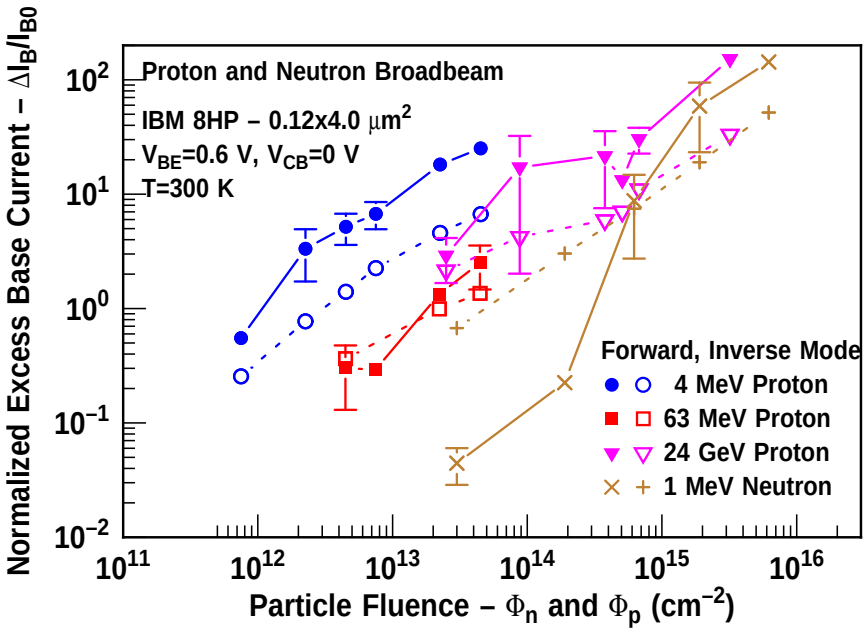

Figure 43: Forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}$ vs. Φ_P and Φ_N for 3rd-generation HBTs irradiated with 1 MeV neutrons, 4 MeV protons, 63 MeV protons, and 24 GeV protons.

Particle energy loss to ionization processes was simulated in SRIM for 4 MeV, 63 MeV, and 24 GeV protons and is plotted as a function of vertical depth into the layers of the

3rd-generation technology platform in Figure 44. A comparison of Figures 37 and 44 clearly indicates that the amount of energy lost by protons, as a result of ionization, to Si and SiO_2 is inversely proportional to proton energy. Although the larger proton LETs at lower energies are consistent with the increases in $\frac{\triangle I_B}{I_{B0}}$ as the proton energy is decreased from 63 to 4 MeV, the significantly larger $\frac{\triangle I_B}{I_{B0}}$ at 24 GeV is inconsistent with the proton LET trends. One plausible explanation for this anomaly is the fact that carrier recombination following proton irradiation at 24 GeV is best described using the geminate model. Therefore, even though fewer initial e-h pairs are created with 24 GeV protons, the final charge yield may not be as small as expected if the carrier recombination rate also decreases, as is predicted by the geminate model. It may even be possible that the reduction in carrier recombination is of greater impact than the initial e-h pair density, which would explain the increase in $\frac{\triangle I_B}{I_{B0}}$ at 24 GeV.

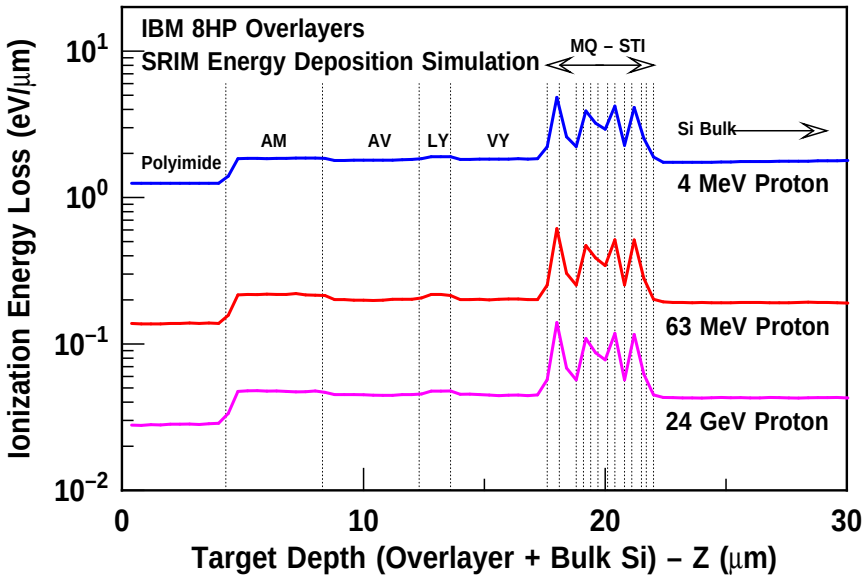

Figure 44: SRIM simulation of the ionization energy loss in the metal and dielectric layers of the 3rd-generation technology platform.

4.3.3 Displacement Damage Factors

The dependence of proton-induced degradation in SiGe HBTs on proton energy can be examined using the *displacement damage factor* (K). Atomic displacement in BJTs reduces the current gain by shortening the minority carrier lifetime [22]. It is therefore

possible to define a damage factor associated with the proton-induced reduction in current gain according to the Messenger-Spratt equation [319]:

$$\frac{1}{\beta(\phi)} = \frac{1}{\beta_0} + K\phi, \tag{95}$$

where β_0 is the initial current gain and Φ is the particle fluence. From a measurement perspective, K can be extracted from the slope of a plot of the reciprocal current gain $\left(\frac{1}{\beta}\right)$ as a function of particle fluence over a range of bias currents. To be sure, ionization in a proton environment distorts the linear relationship between $\frac{1}{\beta}$ and Φ. To account for these effects, the slope of $\frac{1}{\beta}$ as a function of the equivalent gamma fluence (Φ_γ) is subtracted from the slope of $\frac{1}{\beta}$ as a function of Φ_p. The gamma fluence is obtained by dividing the dose by an energy-dependent fluence-to-dose conversion factor ($\frac{D}{\Phi}$) for photons, which has a value of 5×10^{-10} at 1.2 MeV [16]. In Figure 45, the proton (K_p) and neutron (K_n) displacement damage factors are plotted as a function of J_C for 3rd-generation HBTs.

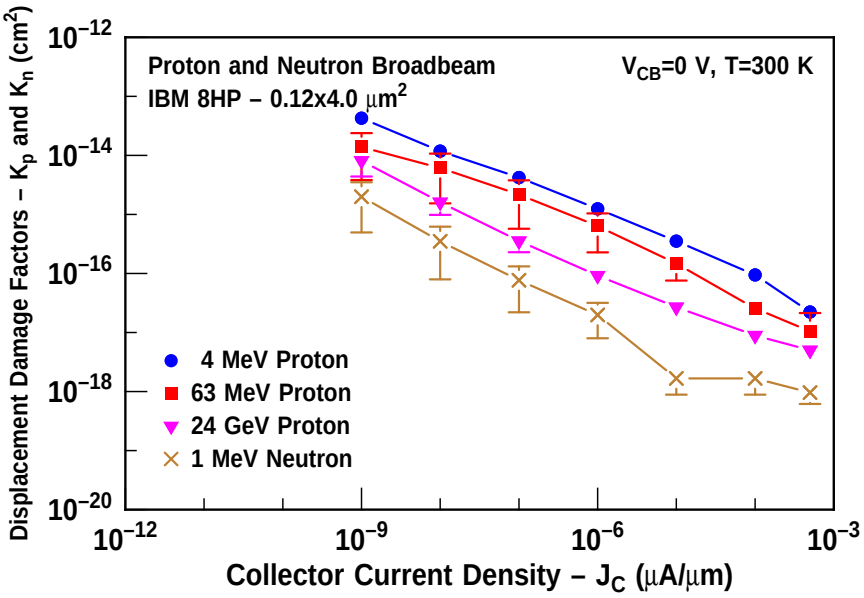

Figure 45: K_n and energy-dependent K_p vs. J_C for 3rd-generation HBTs irradiated with 1 MeV neutrons, 4 MeV protons, 63 MeV protons, and 24 GeV protons.

Each data point represents the average damage factor for two transistors with an A_E of 0.12×4.0 μm^2, and the error bars represent the maximum and minimum bounds on the data. Driven by the bias-dependent reductions in $\Delta\beta$ ($\beta_\Phi - \beta_0$), K_p and K_n both decrease by over three orders of magnitude as J_C is increased from 10^{-9} to 10^{-3} μA/μm^2. Moreover,

as the proton energy is decreased from 24 GeV to 4 MeV, K_p increases. In Figure 46, $\frac{K_p}{K_n}$ is plotted as a function of proton energy for 1st- and 3rd-generation HBTs. Also illustrated in Figure 46 is the ratio of the proton NIEL to the neutron NIEL. As the proton energy is reduced from 24 GeV to 4 MeV, $\frac{K_p}{K_n}$ increases by over 500% for 3rd-generation HBTs, but there is little change in $\frac{K_p}{K_n}$ for 1st-generation HBTs as the energy is decreased from 24 GeV to 63 MeV.

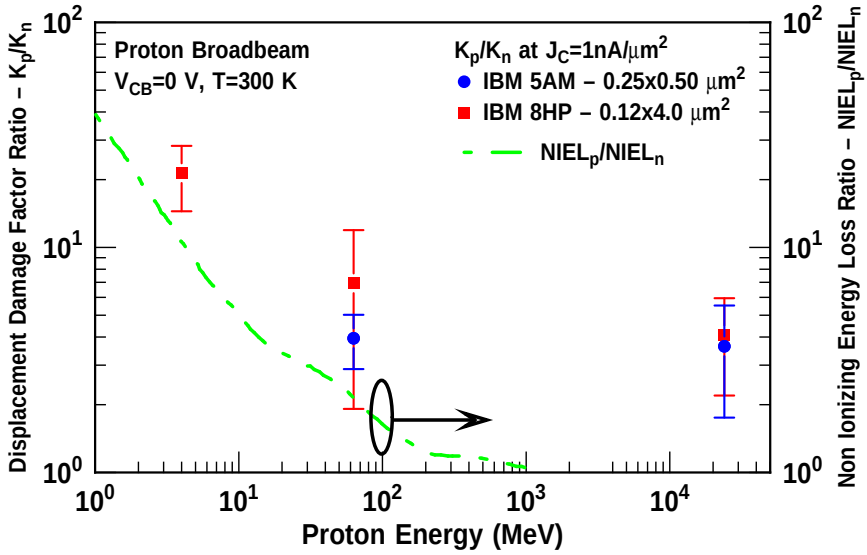

Figure 46: $\frac{K_p}{K_n}$ vs. proton energy for 1st- and 3rd-generation HBTs.

As shown in Figure 47, the NIEL of neutrons to Si (and SiO_2) decreases with decreasing neutron energy, while the NIEL of protons increases with decreasing proton energy. Although the trends in $\frac{K_p}{K_n}$ as a function of proton energy follow the observed variation in the NEIL ratios, $\frac{K_p}{K_n}$ is consistently higher than the NIEL ratio at the three proton energies considered. This discrepancy is a result of the ionization component of proton-induced degradation, which cannot be fully accounted for even after damage factors resulting from 1.2 MeV ^{60}Co gamma irradiation are subtracted from K_p. Furthermore, the difference between $\frac{K_p}{K_n}$ and the NIEL ratio decreases as the proton energy is reduced. This trend is consistent with the relationship between proton LET and energy illustrated in Figure 37.

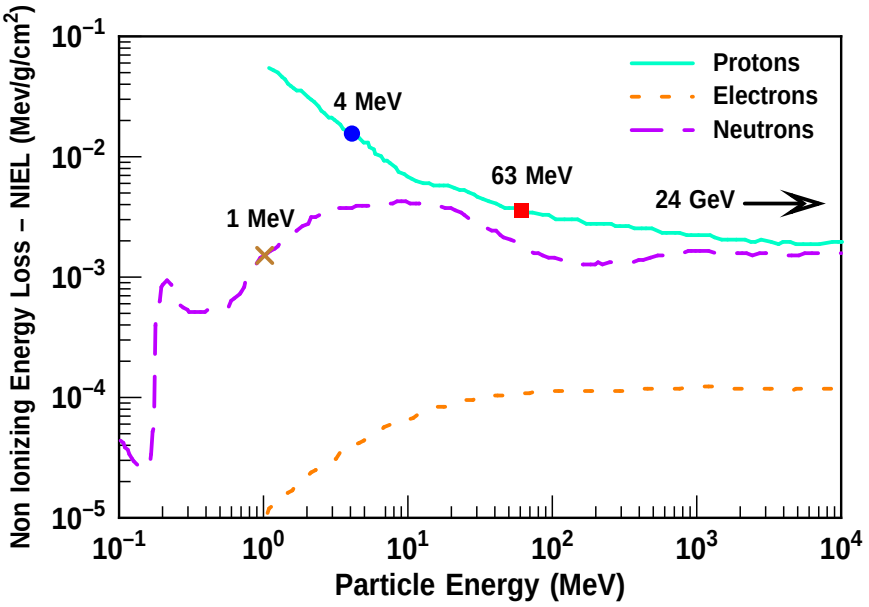

Figure 47: Proton-, electron-, and neutron-induced NIEL vs. particle energy.

4.3.4 Ionization Saturation Phenomena

The gamma-induced $\frac{\triangle I_B}{I_{B0}}$ is plotted as a function of equivalent dose for 1st- and 3rd-generation HBTs in Figure 48. Beginning at a dose of 6 Mrad(SiO_2), the saturation of $\frac{\triangle I_B}{I_{B0}}$ is clearly evident in the inverse-mode response of 1st-generation HBTs. As the dose is increased, the slope of $\frac{\triangle I_B}{I_{B0}}$ decreases in the forward mode of both platforms and in the inverse mode of the 3rd-generation platform. These changes suggest an onset of saturation in the density of oxide trapped charge and Si/SiO_2 interface traps in the BE spacer and STI oxides of both platforms. The saturation of $\frac{\triangle I_B}{I_{B0}}$ is a direct consequence of the shifting of the SRH recombination peak below the Si/SiO_2 interface.

As described in Section 4.2, surface-SRH recombination is characterized by n_{I_B} values between one and two, while sub-surface SRH recombination is characterized by n_{I_B} values that are greater than two. In Figure 49, the post-irradiation forward-mode n_{I_B}, which is averaged over V_{BE} values ranging from 0.6 V to 0.65 V, is plotted as a function of dose for 1st- and 3rd-generation HBTs. All radiation sources are represented in Figure 49. The conversion of the proton and neutron fluence to an equivalent dose is facilitated using the energy-dependent dose-to-fluence conversion factor. In 1st-generation HBTs, n_{I_B} saturates

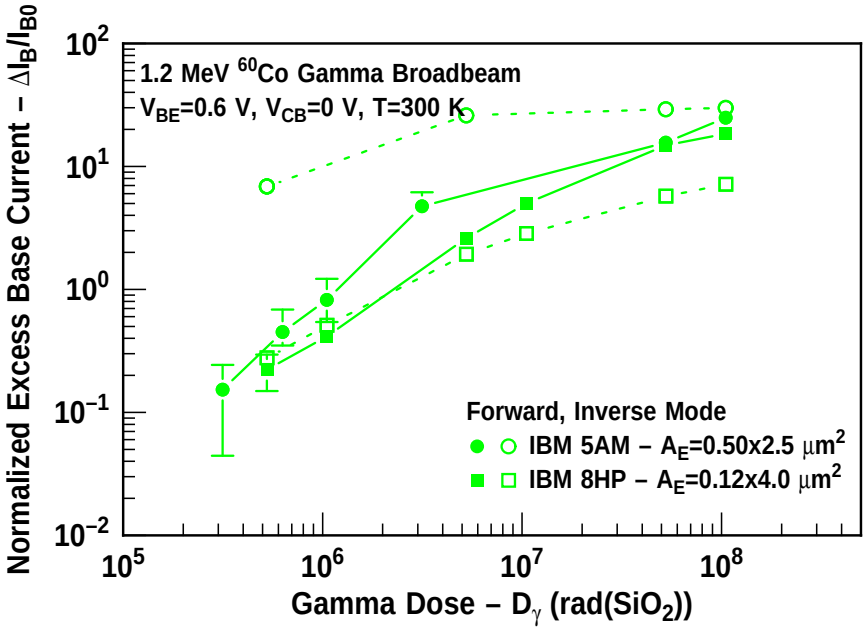

Figure 48: Forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}$ vs. 1.2 MeV ^{60}Co gamma dose for 1$^{\text{st}}$- and 3$^{\text{rd}}$-generation HBTs.

at two for all radiation sources, while in 3$^{\text{rd}}$-generation HBTs, the 24 GeV proton-induced n_{I_B} is greater than two for doses larger than 10 Mrad(SiO_2). These results suggest that the proton- neutron- and gamma-induced $\frac{\triangle I_B}{I_{B0}}$ in 1$^{\text{st}}$-generation HBTs are all dominated by SRH recombination, and that other physical mechanisms, such as BE spacer band-to-band tunneling, dominate the radiation response in 3$^{\text{rd}}$-generation HBTs at these high fluence and energy levels.

Although the radiation-induced saturation in $\frac{\triangle I_B}{I_{B0}}$ has not been previously observed in this technology, recent mixed-mode electrical stress experiments on 1$^{\text{st}}$- and 3$^{\text{rd}}$-generation HBTs have demonstrated that $\frac{\triangle I_B}{I_{B0}}$ becomes increasingly sub-linear in its time dependence as the stress time accumulates [320]. 1.2 MeV ^{60}Co gamma and 10 keV x-ray irradiation on 20 nm n-FETs have also resulted in ΔV_{th} saturation from doses as low as 3 Mrad(SiO_2) and was attributed to pre-irradiation precursors in the SiO_2 that determined the maximum possible interface trap density [321].

The saturation of n_{I_B}, observed for 1.2 MeV ^{60}Co gamma irradiation, can be interpreted as a shift in the peak recombination rate below the Si/SiO_2 interface. For proton and neutron irradiation on 3$^{\text{rd}}$-generation HBTs, n_{I_B} is consistently greater than two, which

may be attributed to a trap-assisted tunneling current in the BE junction, as described in [322]. This tunneling component is expected to increase with HBT scaling as the base width is reduced, the BE spacer is thinned, and the emitter and base doping are increased [323]. These trends are all realized in the scaling of these SiGe HBTs from the 1st- to the 3rd-generation technology platform. With scaling, displacement damage processes now contribute to the radiation-induced $\frac{\triangle I_B}{I_{B0}}$ via the creation of deep-level trap states and the reduction of the potential barrier in high-field regions [324]. These mechanisms have also been used to explain n_{I_B} values that are greater than two at low temperatures [325].

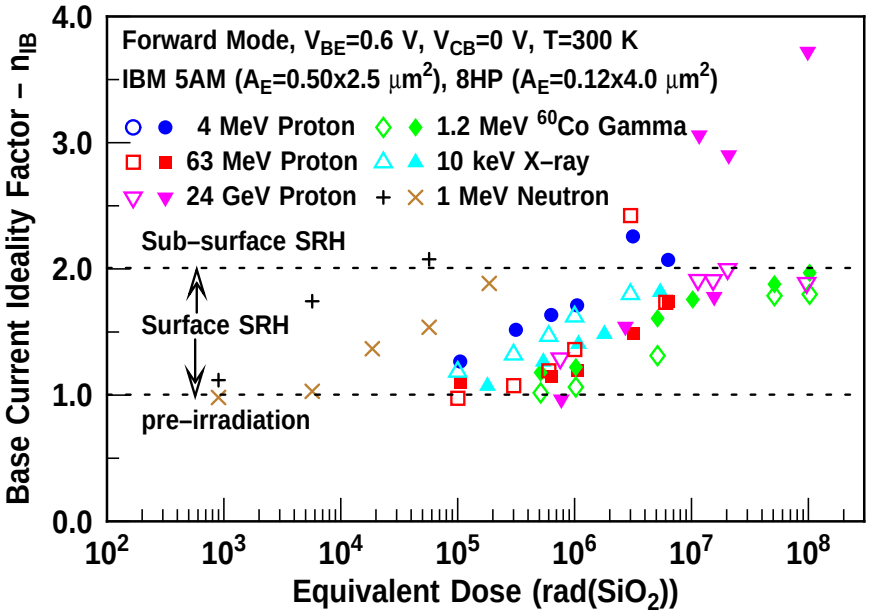

Figure 49: Forward-mode n_{I_B} vs. equivlent dose for 1st- and 3rd-generation HBTs irradiated with 1 MeV neutrons, 4 MeV protons, 63 MeV protons, 24 GeV protons, 10 keV x-rays, 1.2 MeV ^{60}Co gamma rays.

4.3.5 Radiation-Induced Degradation at High Injection

4.3.5.1 Transconductance

Transconductance (g_m) can be used to describe the current drive capability of the transistor and is defined as the relative change in J_C as a function of V_{BE}, which can be expressed as

$$g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{qI_C}{k_B T}. \tag{96}$$

The proton-, neutron- and gamma-induced $\triangle g_m$ ($g_{m,post} - g_{m,pre}$) are extracted from

the forward-mode Gummel characteristics at V_{BE}=0.9 V, and the percentage change in g_m $\left(\frac{100\times\triangle g_m}{g_{m,pre}}\right)$ is plotted as a function of equivalent dose for 3rd-generation HBTs in Figure 50. The average percentage decrease in g_m at the cumulative fluence is 50% for protons, 40% for neutrons, and less than 10% for gamma rays. These large changes in the post-irradiation g_m for protons and neutrons have serious implications for several key performance characteristics such as the emitter-to-collector transit time and the peak cutoff frequency.

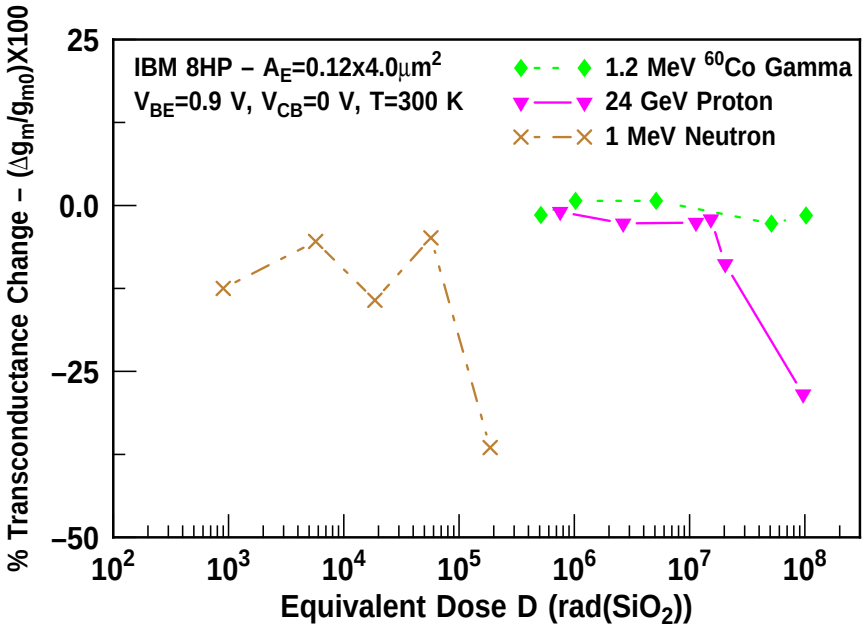

Figure 50: Forward-mode Δg_m vs. equivalent dose for 1st- and 3rd-generation HBTs irradiated with 1.2 MeV ^{60}Co gamma, 24 GeV protons, and 1 MeV neutrons.

4.3.5.2 Collector Resistance

In Figure 51, the high-injection pre- and post-irradiation common-emitter output characteristics at I_B=1 μA are plotted for 3rd-generation HBTs irradiated with 24 GeV protons, 1 MeV neutrons, and 1.2 MeV ^{60}Co gamma rays to cumulative dose values of 94 Mrad(SiO$_2$), 0.2 Mrad(SiO$_2$), and 100 Mrad(SiO$_2$), respectively. At these post-irradiation levels, reductions of up to 74% are observed in I_C for protons and neutrons and up to 50% for gamma rays. The collector resistance in the saturation region ($r_{c,sat}$) is extracted from the reciprocal slope of the common-emitter output characteristics. In Figure 52, the excess collector resistance ($\triangle r_{c,sat}$=$r_{c,sat}(post)$-$r_{c,sat}(pre)$) is plotted for 3rd-generation HBTs

irradiated with protons, neutrons and gamma rays. The pre-irradiation $r_{c,sat}$ is typically between 450 Ω and 600 Ω for these transistors. The proton- and neutron-induced $\triangle r_{c,sat}$ has a super-linear dose dependence, which results in post-irradiation $r_{c,sat}$ values that are on the order of 10^4 Ω, which represents a 1500% increase over the pre-irradiation value. The gamma-induced $\triangle r_{c,sat}$ has a slightly sub-linear dependence, which yields post-irradiation $r_{c,sat}$ values near 10^2 Ω, which represents a 200% increase over the nominal value.

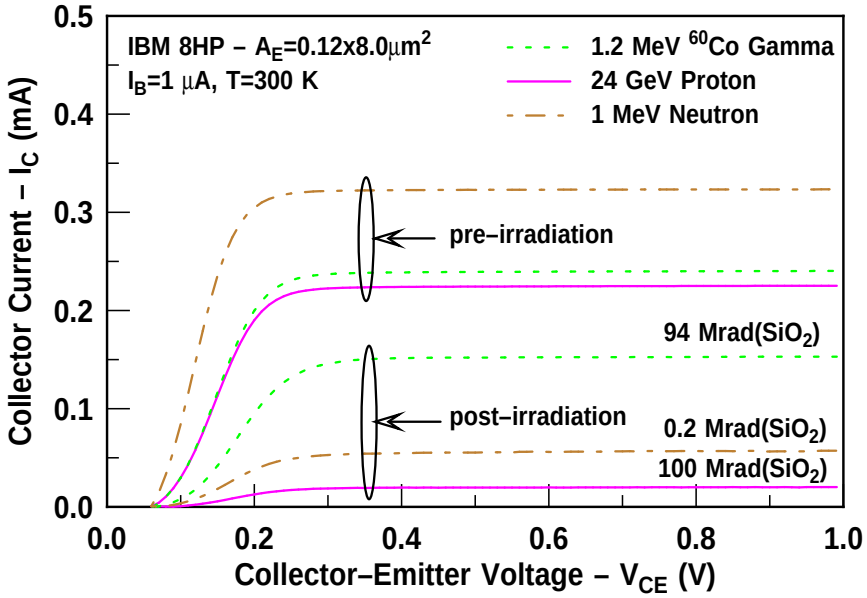

Figure 51: Post-irradiation high-injection output characteristics of 3rd-generation HBTs irradiated with 1.2 MeV ^{60}Co gamma, 24 GeV protons, and 1 MeV neutrons.

The radiation-induced decrease in transconductance and increase in collector resistance are driven primarily by displacement-damage effects such as carrier removal via dopant compensation and reductions in carrier lifetime in the bulk Si. 1.2 MeV ^{60}Co gamma-induced bulk damage has been previously demonstrated using DLTS measurements on silicon detectors irradiated to 200 Mrad(SiO_2) and was attributed to donor compensation levels comparable to a 1×10^{12} n/cm^2 1 MeV neutron fluence [326]. Gamma rays induce displacement damage via the secondary electrons generated from the interactions between photons and the semiconductor lattice [327]. These reactions may explain the mild degradation of $r_{c,sat}$ and g_m following 1.2 MeV ^{60}Co gamma irradiation. Unlike the conventional low-injection ($J_C \approx 1\mu A/\mu m^2$) $\frac{\triangle I_B}{I_{B0}}$ observed at space-relevant doses of a few Mrad(SiO_2), degradation in

$r_{c,sat}$ and g_m have important implications for circuits that operate at bias levels near peak f_T (J_C=10μA/μm^2).

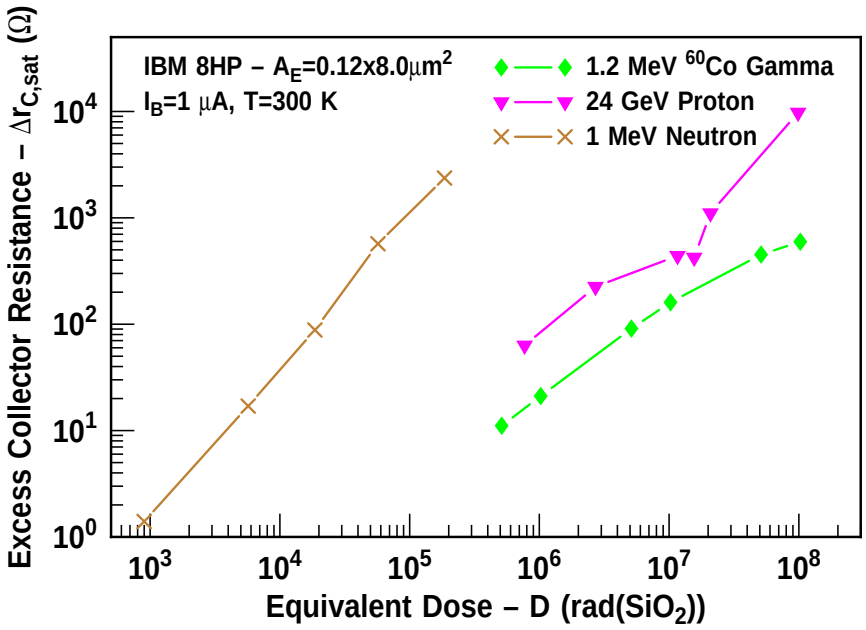

Figure 52: High-injection $\triangle r_{c,sat}$ of 3$^{\text{rd}}$-generation HBTs irradiated with 1.2 MeV ^{60}Co gamma, 24 GeV protons, and 1 MeV neutrons.

4.4 Conclusion

The interaction of radiation-induced G/R traps with the BE and BC junctions in SiGe HBTs has been analyzed via a variety of experiments. Mixed-mode electrical stress measurements across a wide temperature range have demonstrated that fundamental differences in the fabrication of the BE spacer and STI are responsible for the differences in the hot-carrier-induced degradation in the forward and inverse mode [328]. Although electrical stressing yielded no change in the inverse-mode ΔI_B at 85 K in that experiment, a significant forward-mode ΔI_B was observed under identical stress conditions. Similarly, the variations in the forward- and inverse-mode radiation response reported in this chapter indicate that there are fundamentally different trap formation dynamics for the BE spacer and STI Si/SiO$_2$ interfaces.

Several differences in the radiation response of 1$^{\text{st}}$- and 3$^{\text{rd}}$-generation SiGe HBTs to 24 GeV proton, 1 MeV neutron, and 1.2 MeV ^{60}Co gamma irradiation have been presented. For

3^{rd}-generation HBTs, the reduction in the STI thickness and the a novel raised-extrinsic-base structure result in an improved tolerance to 1.2 MeV ^{60}Co gamma irradiation to doses as high as 100 Mrad(SiO_2). A similar result has been observed for 63 MeV proton irradiation, as discussed in [7]. Radiation-induced $\frac{\triangle I_B}{I_{B0}}$ is typically attributed to SRH recombination, which is dominated by midgap trap levels and is characterized by n_{I_B}=1 in the neutral base and $1 \leqslant n_{I_B} \leqslant 2$ in the junction depletion regions [329].

CHAPTER 5

LASER-INDUCED SEU IN HBT DIGITAL LOGIC

5.1 Introduction

The heavy-ion broadbeam and microbeam results presented in [330]-[333] demonstrate that high-speed HBT digital logic is vulnerable to SEEs. In this chapter, an analysis of the error signatures captured during the single-photon pulsed laser irradiation of high-speed HBT digital logic is presented. First, the key aspects of the experimental approach are highlighted with particular emphasis on the parameters of the single-photon pulsed laser system, the custom-designed "Circuit for Radiation Effects Self Test" (CREST), and the block architecture of the 128-bit shift registers contained therein, and the error detection and capture techniques. Second, an analysis of the composition of the laser-induced upsets is presented. Particular attention is paid to the variation in the upset sensitivity as a function of the location of the laser focal spot in the clock tree and the data path. Finally, the impact of power consumption and circuit architecture on the SEU rate in HBT digital logic is discussed.

The results suggest that there are significant variations in the laser-induced SEU response of HBT digital logic as a function of latch architecture, bias conditions, and the spatial location of the laser focal spot. Moreover, the error signatures collected on sensitive transistor nodes and the characteristic upset durations are both in agreement with recently reported heavy-ion microbeam data. This agreement supports the growing credibility of pulsed laser irradiation as a feasible alternative to heavy-ion microbeam irradiation in the determination of the sensitive transistor and circuit nodes and also demonstrates the efficacy of the autonomous error detection approach for high-speed bit error rate (BER) testing.

5.2 Experiment Details

5.2.1 Single-Photon Pulsed Laser Irradiation

Pulsed laser irradiation of 1st-generation HBT digital logic was performed at the NRL facility [221]-[224]. The laser was focused on the topside of the die with a spot size resolution of 0.1 μm. To access sensitive transistors within key circuit blocks, the 1 μm-diameter focal spot must target openings in the thick metal layers at the surface of the die. Any comparison of the results from pulsed laser irradiation and heavy-ion microbeam irradiation requires the definition of an *equivalent laser LET* (L_e). L_e can be written as

$$L_e = \frac{E_p}{d} \int_{r=0}^{+\infty} \int_{z=0}^{d} \int_{t=-\infty}^{+\infty} G_{las}(r,z,t)\, 2\pi r dr dz dt, \tag{97}$$

where G_{las} is the laser-induced generation rate across a classical rectangular parallelepiped (RPP) volume, E_p is the energy required for e-h pair creation (3.6 eV in Si), and d is the thickness of the RPP volume [334]. A summary of the single-photon pulsed laser parameters is provided in Table 4.

Table 4: Single-photon pulsed laser parameters.

Pulse Width	1.0 ps
Wavelength	590 nm (2.1 eV)
Repetition Rate	1 kHz, 10 Hz
Spot Size	1 μm
1/e Penetration Depth	1.8 μm
Data Rate	50 Mbit/s - 6.5 Gbit/s
Pulse Energy	0 - 10 pJ

In practice, the energy deposited into the target is modified by changing the energy of the laser pulse. Correlations of the threshold laser pulse energy to the heavy-ion threshold LET indicate that a laser pulse energy of 1 pJ corresponds to a heavy-ion LET of 3 MeV·cm^2/mg for a wide variety of technologies [221][335]. In this chapter, the energy deposition in the target is presented in terms of the laser pulse energy, which is corrected for reflection from the Si surface. Once a sensitive region is determined in the x-y plane, the laser pulse energy is lowered to its threshold, which is defined as the lowest pulse energy required for single-bit error detection. After the threshold has been determined, the pulse energy is increased

by up to 300% to represent heavy ions, which deposit more energy into the substrate on account of their larger LETs.

5.2.2 Circuit for Radiation Effects Self Test (CREST)

CREST is a NASA self-test circuit (STC) that was designed by the Mayo foundation and fabricated through the MOSIS foundry service [336] on the 1st-generation technology platform [231]. CREST facilitates high-speed BER testing, and efficiently manages error detection and capture in either a self-contained mode or under the control of a Field Programmable Gate Array (FPGA). This FPGA functionality utilizes external ports that are configured for either Low Voltage Differential Signaling (LVDS) or Current Mode Logic (CML). In addition, the FPGA control facilitates the initialization, monitoring, and resetting of CREST during pulsed laser irradiation while reducing the number of high-speed off-chip connections needed to only one – that of a single-ended clock drive [337]. The CREST layout is shown in Figure 53 and the corresponding top-level circuit block diagram is shown in Figure 54.

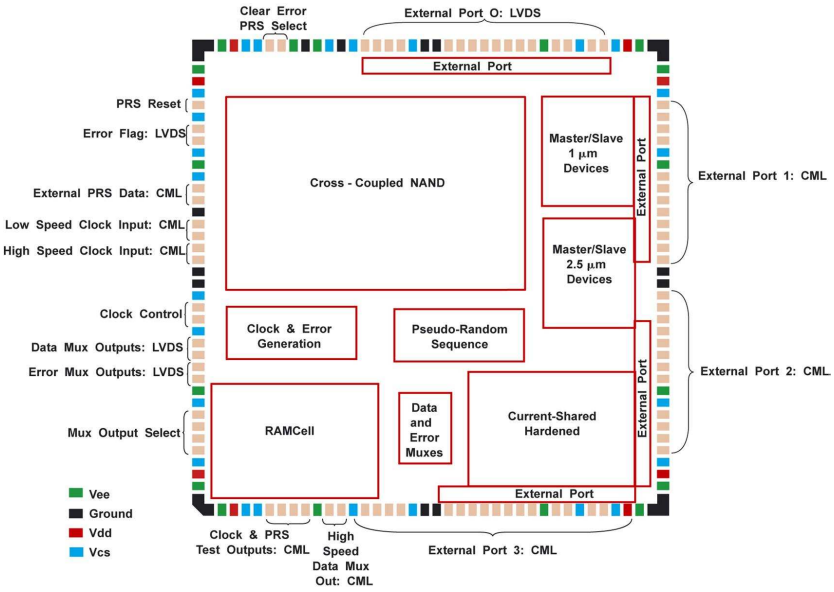

Figure 53: Floorplan of the CREST chip [338].

CREST is composed of four primary functional blocks. These include a pseudorandom sequence (PRS) generator, clock- and error-generation circuitry, nine independent shift

registers, and multiplexing circuitry. In addition to the on-board circuitry, CML input ports are available for an external PRS in addition to high- and low-speed clock inputs, while CML output ports are wired to certain on-board shift registers. Furthermore, dedicated CML and LVDS output ports are available for clock, data, and error signals from selected shift registers, and additional output ports are provided for data output, error output, and error detection signals that are multiplexed from amongst the on-board shift registers. CREST is powered by positive rails at 3.3 V, 1.8 V and a ground rail at 0 V.

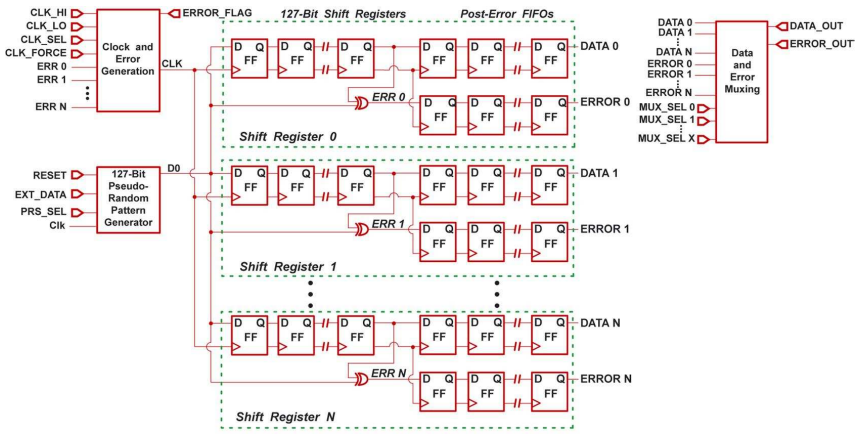

Figure 54: Top-level circuit block diagram of the CREST chip [338].

As shown in Figure 55, the PRS generator is composed of seven cascaded flip-flops and generates a unique sequence that is 2^7-1 bits long. The outputs of the last two flip-flops are fed into an XOR gate, which has its output routed back to the input of the first flip-flop. The PRS generator is enabled via a reset function for pseudorandom initialization, and is also fitted with a multiplexer to switch between the PRS-generated data and an arbitrary external data sequence. The operation of the PRS generator is initiated by setting the flip-flop chains to a static all "1s" state for at least seven clock cycles. This is done by utilizing a reset function, which is initially set high, and once lowered, generates the PRS: 11111110 00000100 00011000 01010001 11100100 01011001 11010100 11111010 00011100 01001001 10110101 10111101 10001101 00101110 11100110 0101010. This PRS contains roughly the same number of "1s" and "0s," and is representative of most data sent over high-speed communication links.

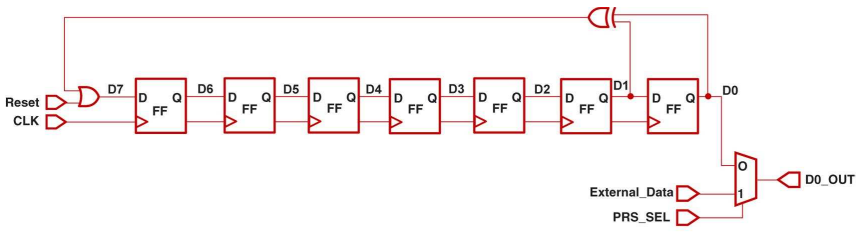

Figure 55: On-board PRS generator of the CREST chip [338].

If the PRS length is equal to the number of stages in a shift register, then during error-free operation the input and output logic states are synchronized, and an error can be easily detected using an XOR gate. A "1" on the output of the XOR gate in any of the shift registers enables the clock control and error detection circuitry, which suspends the high speed operation of CREST and implements the low-speed clock, which is required to capture the correct data and incorrect error streams. Owing to the time required to detect an error and stop the high-speed clock, two additional seven-bit shift registers are used to download the data and error sequences at speeds that are compatible with sub-Gbit/s test equipment. This clock-control circuitry is illustrated in Figure 56.

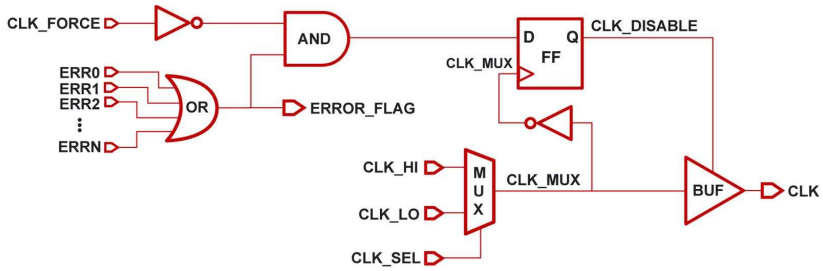

Figure 56: On-board clock control circuitry of the CREST chip [338].

A commercial 12.5 Gbit/s Anritsu MP1764A BERT analyzer was used for data capture. Additional equipment was used to supply and monitor power dissipation, provide diagnostics via an oscilloscope, provide the clock, and condition all signals.

5.2.3 128-Bit Shift Registers

5.2.3.1 Circuit Blocks for Irradiation

The top-level circuit block schematic of the 128-bit shift register is illustrated in Figure 57 with the circuit blocks that are targeted for pulsed laser irradiation highlighted. Single-photon pulsed laser irradiation was performed on the root clock buffers, local clock buffers, and the last flip-flop. A local clock buffer is defined as a buffer that supports a bank of four flip-flops (CLKX4) or two banks of four flip-flops each – for a total of eight (CLK X8). Alternatively, a root clock buffer supports 16 (CLKX16), 32 (CLKX32), or 64 (CLKX64) flip-flops. Root clock buffers are placed earlier in the clock tree, while local clock buffers are placed throughout the shift register. Although all nine registers share identical clock trees, they employ different CML-based latch architectures.

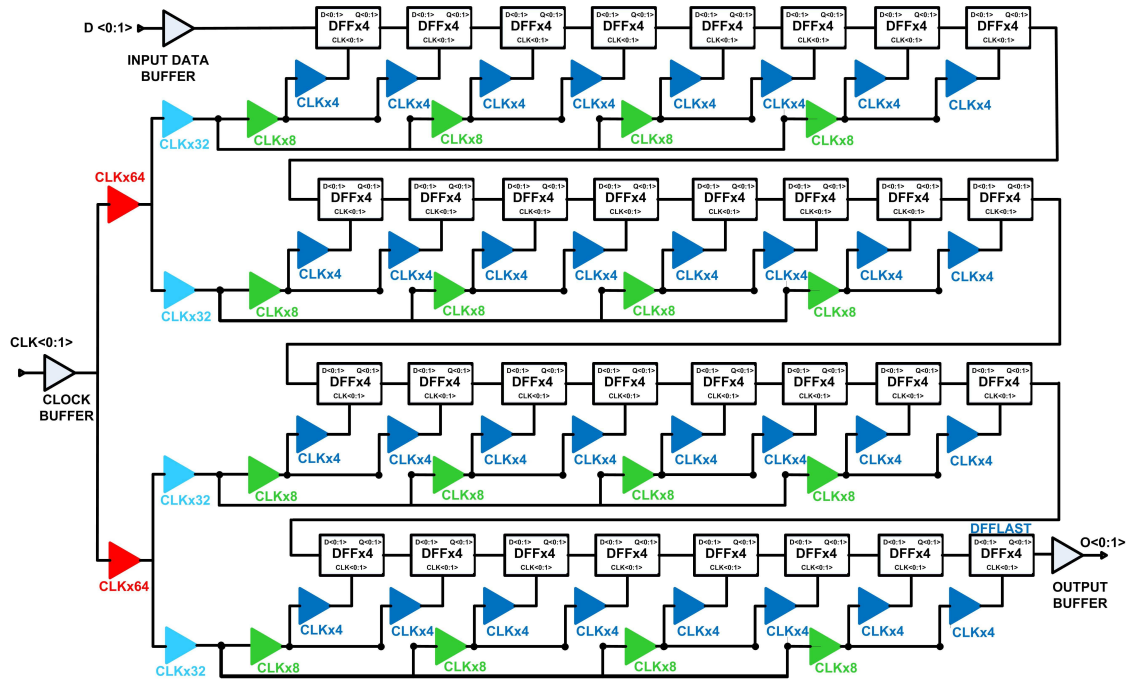

Figure 57: Generic top-level schematic of a 128-bit shift register.

5.2.3.2 Latch Architectures

Five of the nine on-board shift registers are investigated in this chapter. These include the low- and high-power versions of the standard master-slave (LP Std M/S and HP Std

M/S) latch, the current shared hardening (CSH) latch [339], the dual-interleaved (DI) latch [340], and the cross-coupled NAND latch. The latch- and register-level area and power consumption for each architecture are shown in Table 5. The A_E of the transistors used in the latches and the tail current (I_{TAIL}) of the latches were chosen to facilitate transistor switching speeds at values close to peak f_T.

Table 5: Flip-flop- and register-level area and power consumption.

Architecture	Flip-Flop		128-bit Register	
	Area(mm^2)	I_{TAIL}(mA)	Area(mm^2)	Power (W)
LP Std M/S	0.25×1.0	0.60	1.4×1.7	2.97
HP Std M/S	0.25×2.5	1.50	1.4×1.7	3.96
CSH [339]	0.25×1.0	0.60	2.9×2.3	6.27
DI [340]	0.25×2.5	3.00	2.3×1.7	4.95
NAND	0.25×1.0	0.60	3.4×2.4	6.93

The architecture used for local and root clock buffers in all shift registers is depicted in Figure 58. All clock buffers are unhardened and pulsed laser irradiation of any of the transistors Q_1, Q_2, or Q_3, generates upsets, however, only transistor Q_3, which controls I_{TAIL}, was targeted for pulsed laser irradiation.

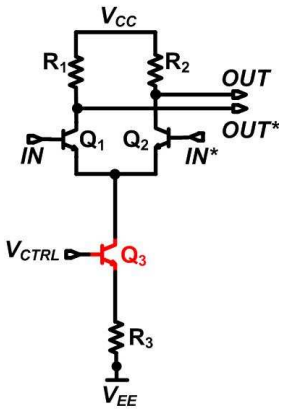

Figure 58: Transistor-level schematic of the CML clock buffer.

The standard master-slave latch architecture is shown in Figure 59. This architecture is composed of a pass cell (Q_1 and Q_2), a storage cell (Q_3 and Q_4), a clocking stage (Q_5 and Q_6), and a voltage-controlled current source (Q_7). A flip-flop is realized by simply cascading two latches (master and slave) in series and alternating the polarity of the clock

signal that is fed into the base terminals of Q_5 and Q_6. An identical architecture is used for the high- and low-power versions, and the variation in power consumption is obtained by simply adjusting the values of R_1 and R_2. The SEU vulnerability of this circuit is rooted in the cross coupling of transistors Q_3 and Q_4 in the storage cell, which affects both output nodes (OUT and OUT*).

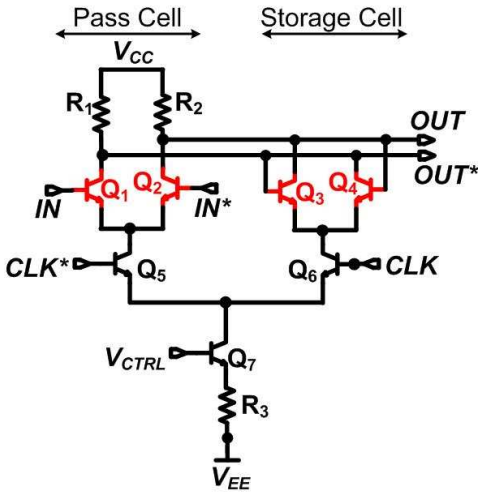

Figure 59: Transistor-level schematic of the low- and high-power standard master-slave latch.

The latch is first considered to be in a hold state defined as "A." In this state, the positive data input (IN) is high (0 V), the negative data input (IN*) is low (-0.3 V), the positive clock input (CLK) is high (-0.7 V), the negative clock input (CLK*) is low (-1.0 V), the positive data output (OUT) is high (0 V), and the negative data output (OUT*) is low (-0.3 V). Pulsed laser irradiation of Q_3, which is "off" in this state, drives OUT low because of the influx of laser-generated electrons into the collector of Q_3 and the subsequent current transient flowing from V_{CC} through R_2 [341]. Moreover, transistor Q_4 is turned off since its base terminal is also connected to OUT, and when Q_4 is turned off, the OUT* node goes high. The switching of the OUT and OUT* logic states constitutes an upset. Furthermore, the load-dependent duration of the current and voltage transients can be as long as 10 ns, which then results in upsets that can easily span several clock cycles during circuit operation at multi-Gbit/s data rates. If the clock polarity is switched so that CLK

is now low (-1.0 V) and CLK* is now high (-0.7 V), then the current transient is simply directed through the pass cell to the negative rail. Data in this chapter is presented for the pulsed laser irradiation of Q_1 and Q_2, in the master latch, and Q_4 , in the slave latch.

The implementation of circuit- and system-level spatial redundancy with the requisite voting circuitry, is an efficient technique for SEE mitigation in HBT digital logic. One such example of this approach is the triple modular redundant (TMR) architecture, in which given circuit is replicated three times and the final output is determined by voting circuitry [342]. Clearly, this technique carries a significant area and power penalty.

The CSH latch architecture uses a similar approach, but at the transistor level, where the power penalty is reduced and voting circuitry eliminated [339]. The CSH latch is realized by simply replacing each transistor in the standard master-slave latch with multiple transistors (three in this example). The multiple transistors are connected in parallel and share common base and collector terminals, as shown in Figure 60.

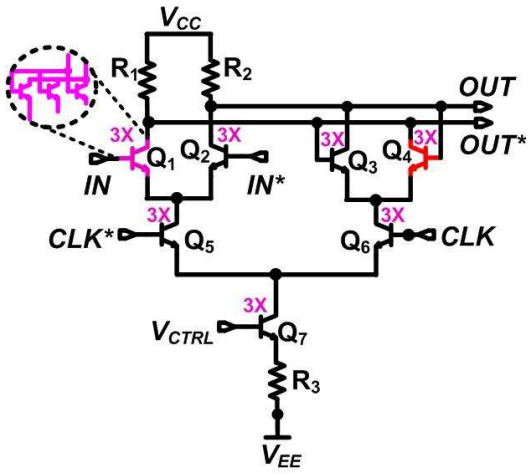

Figure 60: Transistor-level schematic of the CSH latch.

The three parallel-connected transistors in the CSH latch are functionally equivalent to a single transistor in the Std M/S latch. In the Std M/S latch, I_{TAIL} is steered through Q_3, but in the CSH latch, I_{TAIL} is now distributed amongst Q_{3A}, Q_{3B}, and Q_{3C}. In the Std M/S latch, pulsed laser irradiation of Q_3 effectively steers I_{TAIL} from the R_2 branch to the R_1 branch, whereas in the CSH latch, the voltage transient on the collector node of

Q_{3A} is not sufficiently large to steer I_{TAIL} from R_2 to R_1, assuming that Q_{3B} and Q_{3C} do not generate upsets. Data in this chapter is presented for pulsed laser irradiation of Q_4 in the slave latch of the last flip-flop in the CSH shift register.

The DI latch implements redundancy at the latch level by using duplicate copies of the pass and storage cells of the Std M/S latch. Compared to the Std M/S latch, this approach reduces the cross coupling of Q_5 and Q_6 since the base of Q_6 is connected to a different pass cell than the collector of Q_5, as shown in Figure 61. The same holds true for transistors Q_7 and Q_8.

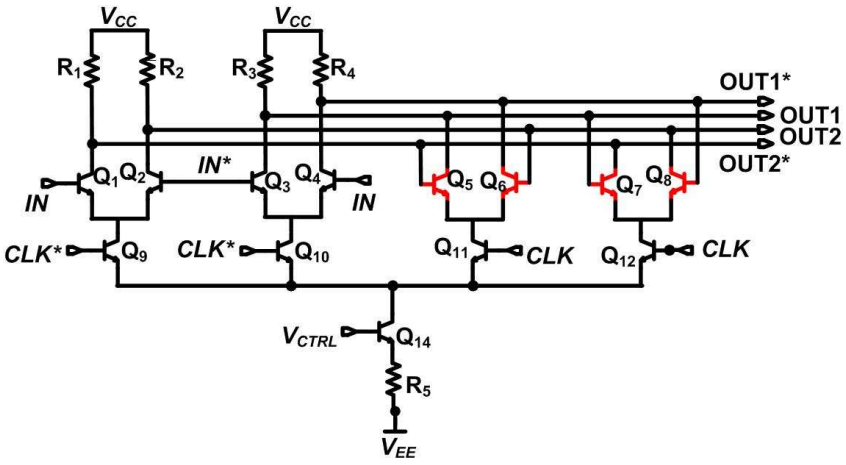

Figure 61: Transistor-level schematic of the DI latch [340].

The same analysis that was presented for the Std M/S latch is now repeated for the DI latch. The latch is again assumed to be in hold state "A," and all node voltages are identical to those described for the Std M/S latch. Unlike the Std M/S latch, the DI latch has duplicate output nodes (OUT1=OUT2 and OUT1*=OUT2*). In this state the positive data input (IN) is high (0 V), the negative data input (IN*) is low (-0.3 V), the positive clock input (CLK) is high (-0.7 V), the negative clock input (CLK*) is low (-1.0 V), the positive data output (OUT1=OUT2) is high (0 V), and the negative data output (OUT1*=OUT2*) is low (-0.3 V). If transistor Q_5 is upset, OUT1 goes low and turns Q_7 on, which sends OUT2* high and reinforces the low on OUT1. During this process, if neither Q_6 nor Q_8 is upset, then OUT2 and OUT1* are maintained at their correct levels. OUT1 and OUT2 are added at the input of the next flip-flop, resulting in a reduction in

the number of upsets.

Flip-flop functionality can also be achieved using a network of cross-coupled NAND2 and NAND3 gates as shown in Figure 62(a). This approach eliminates the transistor-level cross coupling and positive feedback of the other designs. A CML-based implementation of a NAND2 gate is shown in Figure 62(b).

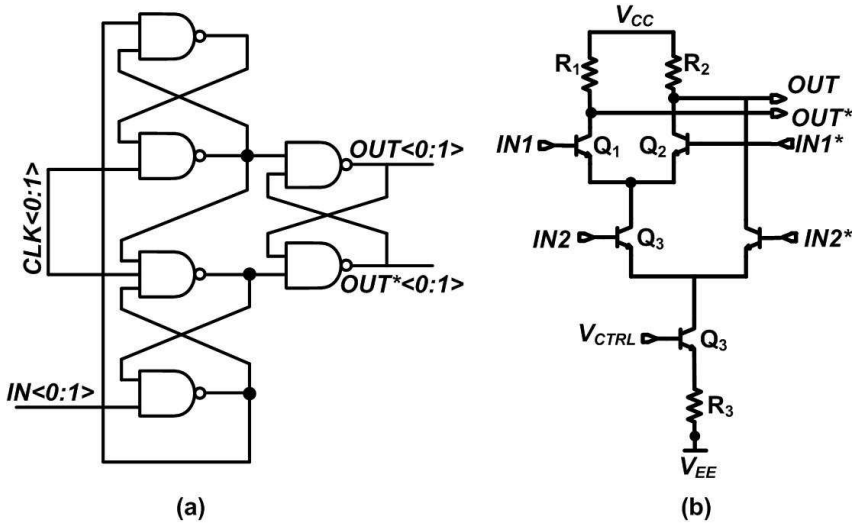

Figure 62: (a) Gate- and (b) transistor-level schematic of the cross-coupled NAND flip-flop.

5.2.4 Error Detection and Capture

Error events were recorded as a 128-bit sequence in which correct bits were represented as either a "1" or a '0,' and incorrect bits were represented as either a "+," which represents a 0→1 (ZTO) transition, or a "-," which represents a 1→0 (OTZ) transition. The laser repetition rate, laser power, data rate, and the number of bit upsets were logged in a data file for each error event. These data files were then processed using a C++ application to generate histograms of the number of bits-in-error (BIE), the error length (EL), the number of 1→0 transitions, and the number of 0→1 transitions. Strictly speaking, BIE is defined as the sum of all "+" and "-" bit errors, and EL is defined as the difference between the bit position of the last and first incorrect bits of the error event. A sample BIE histogram for pulsed laser irradiation of a clock buffer in the Std M/S register at a data rate of 3 Gbit/s and a laser pulse energy of 4.5 pJ is illustrated in Figure 63.

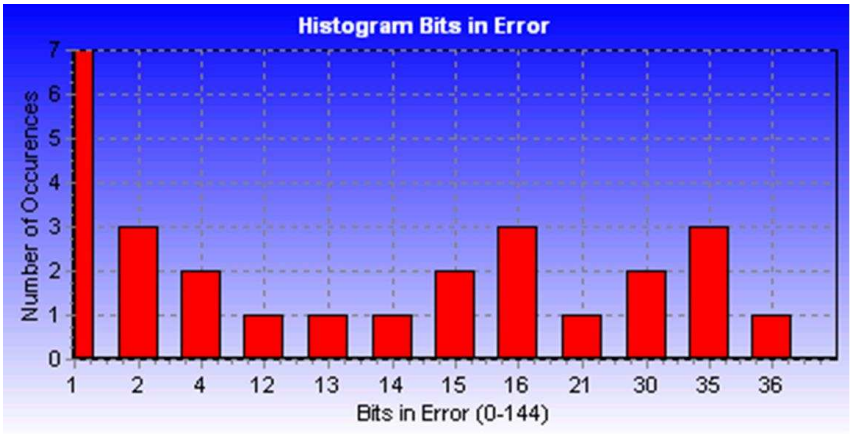

Figure 63: Histogram of the average BIE of a root clock buffer in the low-power standard master-slave shift register operating at 3 Gbit/s for pulsed laser irradiation at 4.5 pJ.

Table 6: Categories for analyzing of pulsed-laser-induced error signatures.

Error Type	Description
Misfire	BIE=0 (a hit on error flag and/or clock-control circuitry)
D0	BIE=2 and EL=128 (two single bit flips separated by 128-bits)
Single bit	BIE=1
XOR	A subset of Single-Bit errors
Flatten to 0	Multiple-bit errors (all incorrect bits '-,' all correct bits 0)
Flatten to 1	Multiple-bit errors (all incorrect bits '+,' all correct bits 1)
LTOT	$\ggg$10% to $\lll$25% of bits are in error vs. expected 50%
MBD0	Multiple bit D0, similar to D0 except it is repeated
Single shift	Pattern changes and never changes back. PRN hit
Multi shift	Best attempt to describe the error as multiple shifts
Double shift	Pattern changes, then changes back
Mangle	Totally scrambled un intelligible errors

The error events can be categorized into 12 categories, as shown in Table 6. For good error statistics, it is desirable to collect at least 100 error events per run, and depending on the circuit and laser parameters, there can be significant variation in the length of time required for each run. This variation in the run time means that the data files contain a randomly distributed number of error events. Therefore, in order to accurately compare the recorded events, BIE, EL, OTZ, and ZTO must all be normalized by the number of error events in each log file.

5.3 Error Signature Analysis

5.3.1 Clock Buffer Sensitivity

The primary figures of merit to be used in comparing the relative sensitivity of different latch architectures and bias configurations are the average BIE, single-bit error percentage (SB%), and the percentage of 1→0 transitions. In Figure 64, the average BIE is plotted as a function of laser pulse energy for all clock buffers in the LP Std M/S register. These errors originate from transistor Q_3 in the local and root clock buffers at data rates of 1 Gbit/s and 6.5 Gbit/s.

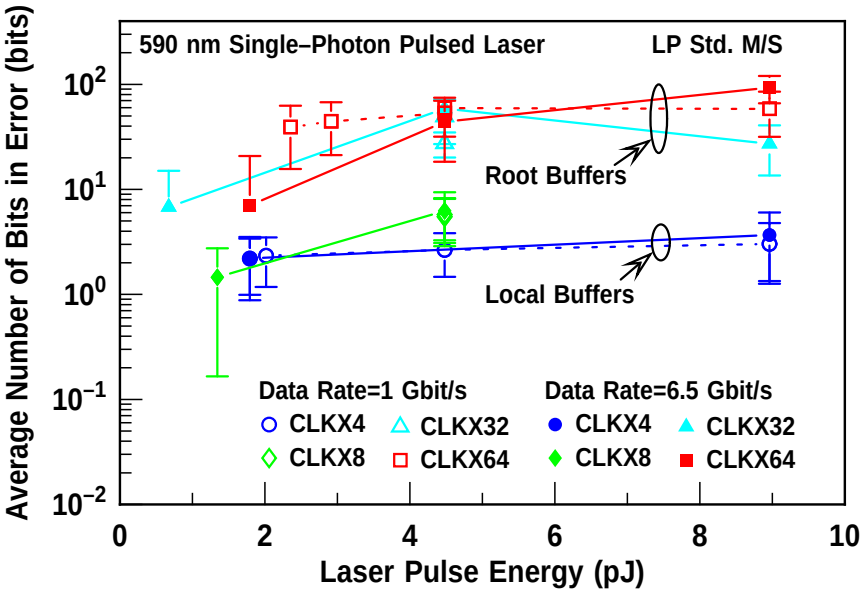

Figure 64: Average BIE vs. laser pulse energy for local and root clock buffers in the low-power standard master-slave shift register operating at 1 Gbit/s and 6.5 Gbit/s.

Pulsed laser irradiation of the local clock buffers results in a low average BIE, regardless of the data rate or pulse energy. Conversely, for root clock buffers, the average BIE is over an order of magnitude higher than for local clock buffers. This result is a direct consequence of the fact that upset currents originating from the OUT node in Figure 58 are propagated through many more flip-flops for a root clock buffer, than for a local clock buffer. Nevertheless, it should be noted that the register architecture mandates that there are many more local than root clock buffers, which in a heavy-ion broadbeam environment increases the contribution of upsets originating from the local clock buffers to the overall

SEU rate. The average BIE is plotted as a function of data rate in Figure 65 for all clock buffers at laser pulse energies of 4.5 and 9.0 pJ, and the increase in the average BIE that was observed for root clock buffers, as compared to local clock buffers, is present across all data rates.

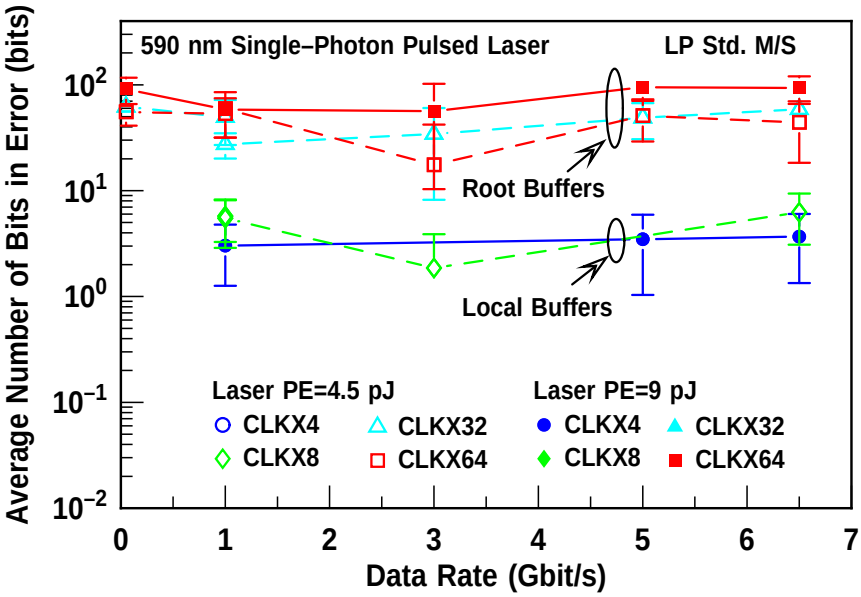

Figure 65: Average BIE vs. data rate at laser pulse energies of 4.5pJ and 9 pJ for local and root clock buffers in the low-power standard master-slave shift register.

Pulsed laser irradiation on both the local and root clock buffers results in an equivalent number of $1 \rightarrow 0$ and $0 \rightarrow 1$ transitions, as depicted in Figure 66. This result is a direct consequence of the fact that transistor Q_3, in Figure 58, is located one level below the differential pairs that switch the clock polarity. The equivalent circuit that is used to simulate heavy-ion-induced upset currents also predicts a drop in the collector voltage at the affected node [335], which if applied to transistor Q_3 in Figure 58, will upset both Q_1 and Q_2 and cause the same number of $1 \rightarrow 0$ and $0 \rightarrow 1$ transitions.

5.3.2 Flip-Flop Sensitivity

Pulsed laser irradiation was performed on the last flip-flop shown in Figure 57 and targeted transistors Q_1 and Q_2 in the pass cell of the master latch and transistor Q_4 in the storage cell of the slave latch. The percentage of $1 \rightarrow 0$ transitions during the pulsed laser irradiation of Q_1 and Q_2 is illustrated in Figure 66.

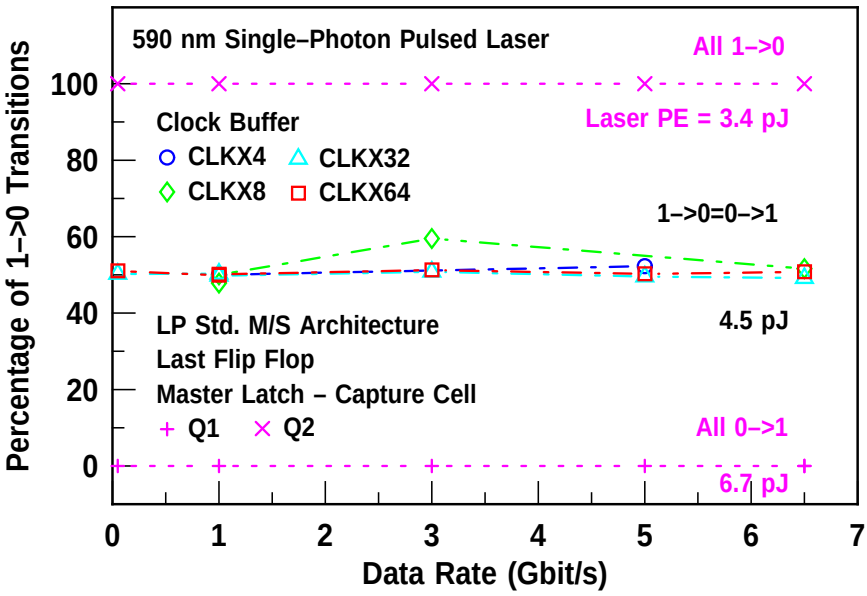

Figure 66: Percentage of $1 \rightarrow 0$ transitions vs. data rate at laser pulse energies of 3.4 pJ, 4.5 pJ, and 6.7 pJ for flip-flops and clock buffers the low- and high-power standard master-slave shift register.

At a laser pulse energy of 6.7 pJ, irradiation of Q_1 in Figure 59 results in a data pattern that is composed of all "1s," which corresponds to the "Flatten to 1" error in Table 6. Pulsed laser irradiation of Q_2, this time at a laser pulse energy of 3.4 pJ, results in a data pattern that is composed of all "0s," which corresponds to the "Flatten to 0" error in Table 6. The opposing polarity of the bit streams is a direct consequence of the fact that Q_2 is the complementary transistor to Q_2 in the differential switching pair.

Pulsed laser irradiation of Q_1, Q_2, or Q_3 in Figure 59 results in a drop in the voltage at the corresponding collector nodes. If IN is low ("0"), then the irradiation of Q_1 brings its collector voltage low when it would normally be high. This upset propagates through the circuit and results in a high ("1") on the OUT node when it would normally be low, thereby constituting a $0 \rightarrow 1$ transition. Conversely, if IN is high ("1"), then the irradiation of Q_2 brings its collector voltage low. This propagates through the circuit as a high ("1") on the OUT* node or a low ("0") on the OUT node, thereby constituting a $1 \rightarrow 0$ transition. The above analysis assumes that only the last flip-flop is irradiated, that no other transistors in the last flip-flop are irradiated, and that irradiation is applied to the target transistor for a sufficiently long duration. This complementary flattening behavior is also observed for

pulsed laser irradiation of the last flip-flop in other circuit architectures.

In Figure 67, the average BIE is plotted as a function of data rate for pulsed laser irradiation of transistor Q_3 in the storage cell of the slave latch of the last flip-flop in the LP and HP Std M/S shift registers. The average BIE is compared for I_{TAIL}=0.6 mA and 1.5 mA and at laser pulse energies of 0.7 pJ, 1.6 pJ, 3.4 pJ, and 6.7 pJ. As expected, the last flip-flop exhibits a greater sensitivity to pulsed laser irradiation than local clock buffers. This is evidenced by the fact that the average BIE for Q_3 in Figure 59 is ten to 15 bits at the highest data rate and pulse energy, as shown in Figure 67. This is in contrast to the average BIE for Q_3 in Figure 58 for a local clock buffer at similar data rate and pulse energy, which is between two and three bits as shown in Figure 65. Additionally, at pulse energies above the threshold, the average BIE for pulsed laser irradiation of Q_3 in Figure 59 steadily increases as a function of data rate, which is characteristic of a particularly short upset duration.

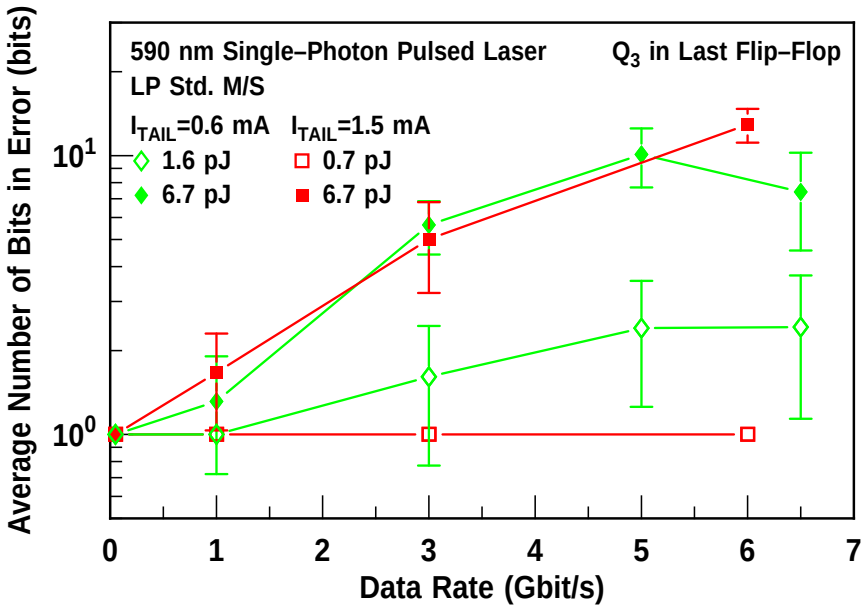

Figure 67: Average BIE vs. data rate at I_{TAIL}=0.6 mA and 1.5 mA and at laser pulse energies of 0.7 pJ, 1.6 pJ, and 6.7 pJ for the slave latch in the last flip-flop of the low- and high-power standard master-slave shift registers.

Also shown in Figure 67 is the bias dependence of the laser-induced upsets. In the last flip-flop, there was no improvement in the average BIE as I_{TAIL} is increased. Similarly, in both the local and root clock buffers, a very small reduction in the average BIE as a

function of I_{TAIL} was observed, as shown in Figure 68. In the simulations of ion strikes that were performed in [340], as I_{TAIL} was increased, the upset rate decreased since at larger I_{TAIL} values the load resistance on the collector (R_C) must be reduced to maintain the same voltage swing. Therefore, if the radiation-induced upset current originating from the affected transistor remains the same, it must now flow through a smaller R_C, which reduces the upset voltage. In contrast, the experimental results presented here do not support the simulation results in [340]. One possible explanation for this discrepancy is the fact that the simulations in [340] assumed that the upset current originating from the transistor would remain the same when the tail current is increased in the HP Std M/S latch. However, in the experimental results presented here, the HP Std M/S flip-flop is implemented using a larger transistor, and the sensitive volume for charge collection, which is defined by the area enclosed within the DT, is now larger. This larger sensitive volume translates into a larger upset current [332], and compensates for the reduction in R_C.

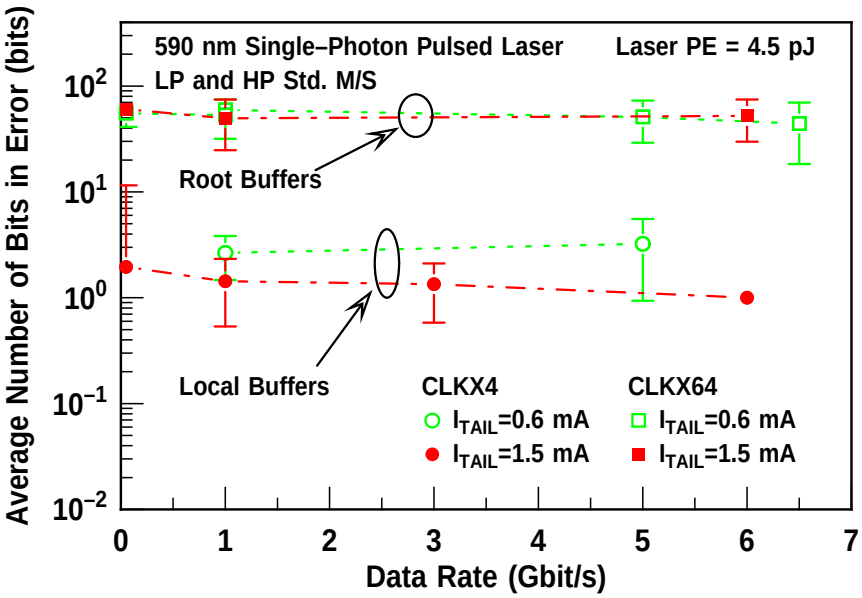

Figure 68: Average BIE vs. data rate at I_{TAIL}=0.6 mA and 1.5 mA and a laser pulse energies of 4.5 pJ for local and root clock buffers of the low- and high-power standard master-slave shift registers.

5.3.3 Impact of Latch Architecture

In the slave latch of the Std M/S architecture, the strong variation in the average BIE as a function of data rate for pulse energies above threshold, which is shown in Figure 67, can be explained by looking closely at the composition of the error signatures. In Figure 69, this is done by plotting a histogram of errors categorized according to their length as single-bit errors, two- to four-bit errors, nine- to 64-bit errors, and 65- to 144-bit errors. This data is presented as a function of data rate for the pulsed laser irradiation of Q_1 and Q_2 in Figure 59 at laser pulse energies of 6.7 pJ and 3.4 pJ. Single-bit errors dominate the response at low data rates, and complex-burst errors become more prominent as the data rate is increased. Therefore, by looking at the SB% as a function of latch architecture further insight into the potential for effective circuit-level SEE mitigation in HBT digital logic can be obtained.

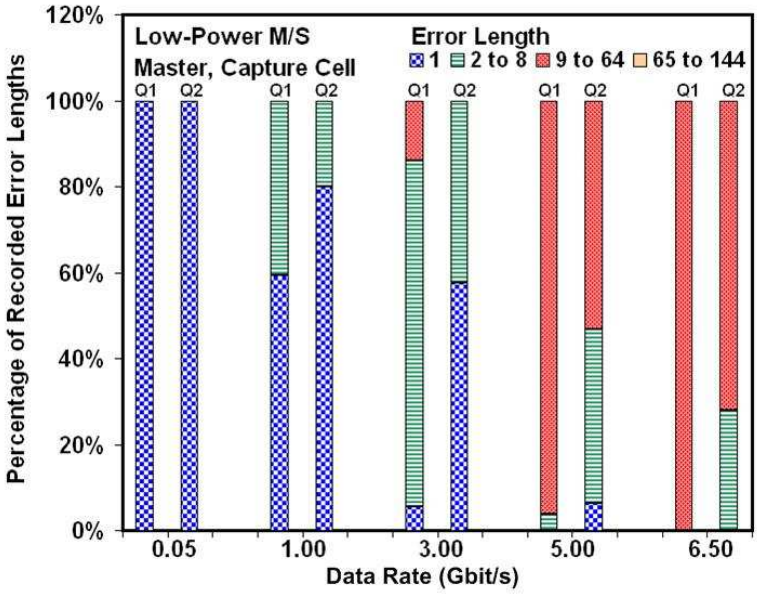

Figure 69: Average error length vs. data rate for transistors Q_1 and Q_2 in the slave latch of the last flip-flop of the low- and high-power standard master-slave shift register.

The average BIE for pulsed laser irradiation of CLKX32 buffers in the LP Std M/S, NAND, CSH, and DI architectures is plotted as a function of laser pulse energy in Figure 70.

Although there is no significant difference in the value at which the average BIE saturates, there is some increase in the threshold laser pulse energy for all hardening techniques. At the lowest data rate, pulsed laser irradiation of the DI shift register produces considerably fewer errors than the LP Std M/S shift register, both below the threshold and in the saturation regime, while the NAND shift register did not yield significant improvement in either region. Finally, pulsed laser irradiation of the CLKX24 buffer in the CSH architecture yields an increase in the threshold laser pulse energy at a data rate of 3 Gbit/s.

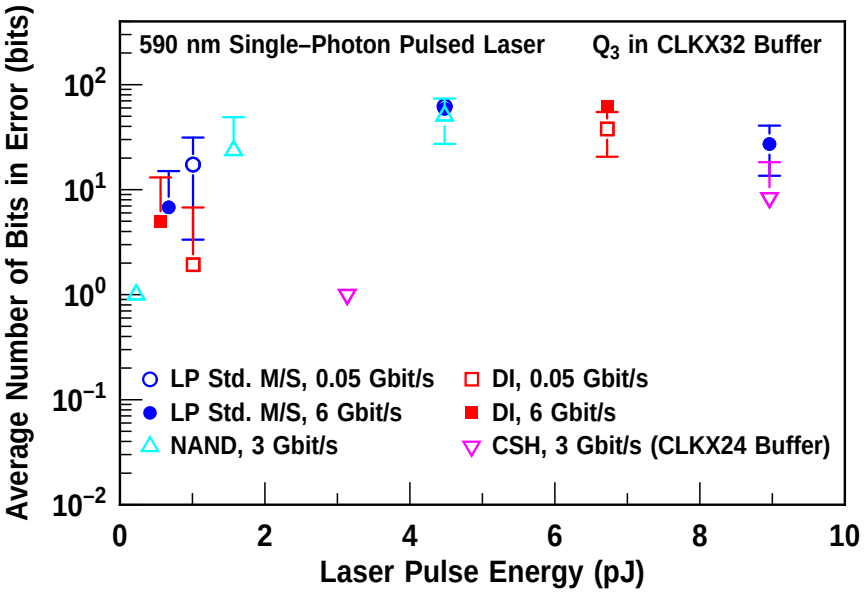

Figure 70: Average BIE vs. laser pulse energy for transistor Q_3 in the root clock buffer (CLKX32) of the low-power standard-master slave, dual-interleaved, NAND, and CSH (CLKX24) shift registers operating at 0.05 Gbit/s, 3 Gbit/s and 6 Gbit/s.

The SB% will now be used as the figure of merit to compare the SEU sensitivity as a function of latch architecture. A larger SB% is indicative of a shorter error length and a smaller average BIE, which at the system level translates into a reduction in the overall SEU rate. The greatest evidence of the SEU mitigation obtained using these circuit-level RHBD approaches is illustrated in Figure 71.

In this figure, the SB% of the LP and HP Std M/S, DI, and CSH architectures is plotted as a function of data rate at pulse energies above threshold. The SB% for both the LP and HP Std M/S falls to below 10% at 3 Gbit/s, while reductions of up to 70% and 90% are observed for the CSH and DI architectures, respectively. These gains are very impressive

and serve as supporting evidence of the promise of circuit-level RHBD for SEU mitigation in HBT digital logic. Moreover, they help to validate the viability of pulsed laser irradiation as a tool for evaluating transistor- and circuit-level RHBD techniques.

Circuit simulations addressing the relative SEU immunity of these latch architectures have been presented in [331][340]. Although the NAND gate architecture was found to have the lowest error rate, its large power consumption and circuit area render it the most undesirable RHBD implementation. In addition, the failure to completely eliminate transistor-level cross coupling in the CSH latch architecture was found to compromise any gains in SEU immunity that were made by the utilization of multiple circuit paths [335].

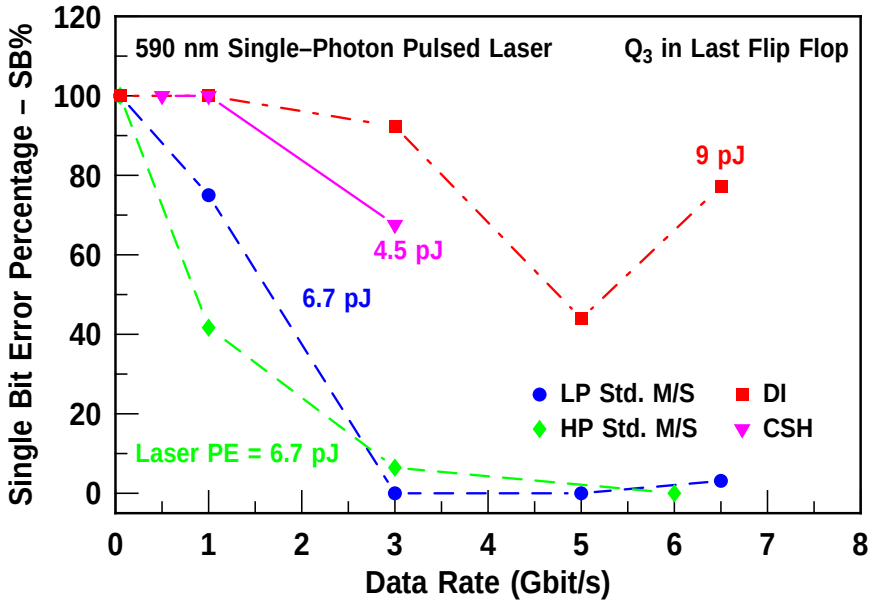

Figure 71: SB% vs. data rate at laser pulse energies of 4.5 pJ, 6.7 pJ, and 9 pJ for transistor Q_3 in the last flip-flop of the CSH, dual-interleaved, low- and high-power standard master-slave shift registers.

5.4 Conclusion

A comprehensive solution to the SEE vulnerability of HBT digital logic will be realized only through careful understanding of pulsed laser irradiation, heavy-ion broadbeam irradiation, heavy-ion microbeam irradiation, TCAD modeling for accurate charge collection dynamics [341], and robust circuit simulation to realize novel architectures. The observed variation in the SB% for the various latch architectures can be coupled to the characteristic

upset duration. In the case of the low-power standard master-slave latch, a characteristic upset duration on the order of 2.3 ns is observed for the capture cell in the master latch, and the corresponding upset duration for the storage cell in the slave latch is 1.13 ns. Both of these values compare well with those obtained in [330]. Interestingly, the upset duration for the last transistor in the storage cell of the slave latch in the DI architecture is on the order of 0.2 ns, which explains the increased SB% in this architecture.

Heavy-ion microbeam irradiation is yet another tool that can be used to explore the sensitive transistor nodes in a circuit. The results of a recent heavy-ion microbeam analysis of 2^{nd}-generation HBT digital logic, which were presented in [343], are very relevant to the results presented in this chapter. In that study, a complementary behavior in the response of transistors in the differential pair of the pass cell of the master latch was also observed, while the transistors of the voltage-controlled current source were found to be less sensitive. Moreover, it was determined that the upset durations in the slave cell were generally shorter than those in the master cell, a result that was attributed to the variation in transistor geometry and switching currents implemented in those latches [343]. A similar result was observed in the data presented in this chapter, even though both the master and slave latches employ the same tail current and transistor geometry.

In this chapter, a comparative study of the SEU sensitivity in 1^{st}-generation 128-bit shift registers has been presented. The effectiveness of a variety of circuit-level RHBD approaches for SEE mitigation was investigated by analyzing the latch-architecture dependence, the bias dependence, and the data path and clock buffer sensitivity. Comparisons of the relative sensitivities of the various latch architectures were facilitated via the classification of the error signatures into descriptive categories.

The results presented in this chapter also indicate that the sensitive nodes in the clock buffers and flip-flops are distributed throughout these shift registers. Irradiation of the root clock buffers results in up to ten times more errors than irradiation of the local clock buffers at laser pulse energies below the threshold. Conversely, at pulse energies above the threshold, there is no significant increase in the number of errors emanating from the root clock buffers. Increases in the tail current, which were previously found to improve SEU

immunity, have no significant effect on the number of errors recorded, and upsets emanating from pulsed laser irradiation on both local and root clock buffers are evenly distributed between 1→0 and 0→1 transitions. Conversely, pulsed laser irradiation of transistors within the differential pair of the standard master-slave latch in the last flip-flop resulted in an asymmetric distribution of errors, which were characterized by a "flattening" of the data to either all "0s" or all "1s." Additionally, at laser pulse energies above threshold, irradiation on these nodes resulted in an increase in the number of errors recorded as a function of data rate. Some improvement in the SEU response is observed for the current shared hardening and dual-interleaved circuit-based RHBD approaches, as compared to the standard master-slave architecture. This difference is only observed when the flip-flops are irradiated but not for irradiation to the local and root clock buffers.

A combination of transistor- and circuit-level RHBD techniques should focus on sensitive nodes within the individual flip-flops and root clock buffers. Moreover, cadence design tools and mixed-mode TCAD can be applied to simulate upsets in these regions, and evaluate the efficacy of various RHBD approaches.

CHAPTER 6

PROTON-INDUCED SEU AT CRYOGENIC TEMPERATURES

6.1 Introduction

In the previous chapter, single-photon pulsed laser irradiation was used to investigate the SEU response of 1st-generation HBT digital logic at room temperature. In this chapter, that investigation is expanded by comparing the SEU response of 3rd-generation HBT digital logic at 300 K to the response at 77 K. First, the impact of the ambient temperature during irradiation on the proton-induced excess base current is evaluated for 1st- and 3rd-generation HBTs using a medium-energy proton source. Next, the mechanisms that enable low-LET medium-energy protons to induce SEEs in HBT digital logic are discussed. Third, the details of the proton and heavy-ion broadbeam radiation experiments are presented, and the corresponding cross sections and error signatures are examined. The chapter is concluded with a presentation of the results from 2-D TCAD simulations and a discussion of the implications for future temperature-dependent SEE testing of HBT digital logic.

The results indicate that the SEU response of HBT digital logic is enhanced at cryogenic temperatures. As the circuits are cooled from 300 K to 77 K, a 300% increase in both the error-event and bit-error cross sections is observed. Moreover, an analysis of the error signatures suggests that there are corresponding increases in the average number of bits-in-error and the average error length over data rates ranging from 50 Mbit/s to 4 Gbit/s. Unlike the multiple-bit errors that are typically observed in a heavy-ion broadbeam environment, single-bit errors dominate the proton-induced SEU response at both 300 K and 77 K. Temperature-dependent measurements of carrier lifetimes in the substrate and calibrated 2-D TCAD simulations both suggest that the increased transistor-level charge collection at cryogenic temperatures, which drives the circuit-level observations, is a mobility-driven

phenomenon. The dual-interleaved latch architecture, which was introduced in Chapter 5, is shown to be very effective in mitigating proton-induced single-event upsets at both 300 K and 77 K. All the results presented here suggest that the ambient temperature of the circuit must be carefully considered during single-event component qualification and indicate the need for heavy-ion broadbeam irradiation at cryogenic temperatures.

6.2 Proton-Induced Ionization at Cryogenic Temperatures

An investigation of proton-induced ionization in SiGe HBTs operating at cryogenic temperatures is a logical pre-requisite to the determination of the low-temperature SEU response of HBT digital logic. In this section, an investigation into the low-temperature transistor-level proton tolerance is facilitated via the irradiation of 1st- and 3rd-generation HBTs in a liquid nitrogen (LN_2) environment.

6.2.1 Experiment Details

Proton irradiation at 63 MeV was performed at the CNL facility [203][204], which is described in Section 2.3.3. Using the procedure described in Chapter 3, several HBTs, configured *dc* test structures, were packaged into 28-pin DIPs. Proton irradiation at 77 K was facilitated by immersing a custom-designed PCB containing these DIPs into an expanded polystyrene (EPS) dewar filled with LN_2. To facilitate accurate temperature comparisons, proton irradiation at 300 K was performed in the same EPS dewar, with the LN_2 removed. According to SRIM calculations, the interaction of 63 MeV protons with LN_2 and EPS results in a 3.9% increase in the proton LET along with a slight increase in transistor temperature. 1st- and 3rd-generation HBTs were irradiated with all terminals grounded, and the pre- and post-irradiation Gummel characteristics were measured using the Agilent 4155 SPA. The 1st-generation HBTs have an A_E of 0.50×1.0 μm^2, while the 3rd-generation HBTs have an A_E of 0.12×2.0 μm^2.

6.2.2 *dc* Performance Degradation

In Figure 72, the pre- and post-irradiation Gummel characteristics of a 1st-generation HBT irradiated to 6 Mrad(SiO_2) at 77 K and 300 K are illustrated. In the pre-irradiation

Gummel, the slope of J_C and J_B increases drastically as the transistor is cooled. This increase in slope is a result of the fact that the intrinsic carrier density (n_i) is exponentially related to the bandgap (E_G), thereby increasing V_{BE} at a fixed-I_C as the temperature is reduced. A trend line at J_C=10 nA/μm^2 is included in Figure 72 to indicate the collector current density at which the post-irradiation $\frac{\triangle I_B}{I_{B0}}$ ($\frac{\triangle I_B}{I_{B0}}\big|_{J_C=10\ \mathrm{nA}/\mu\mathrm{m}^2}$) is compared as a function of temperature.

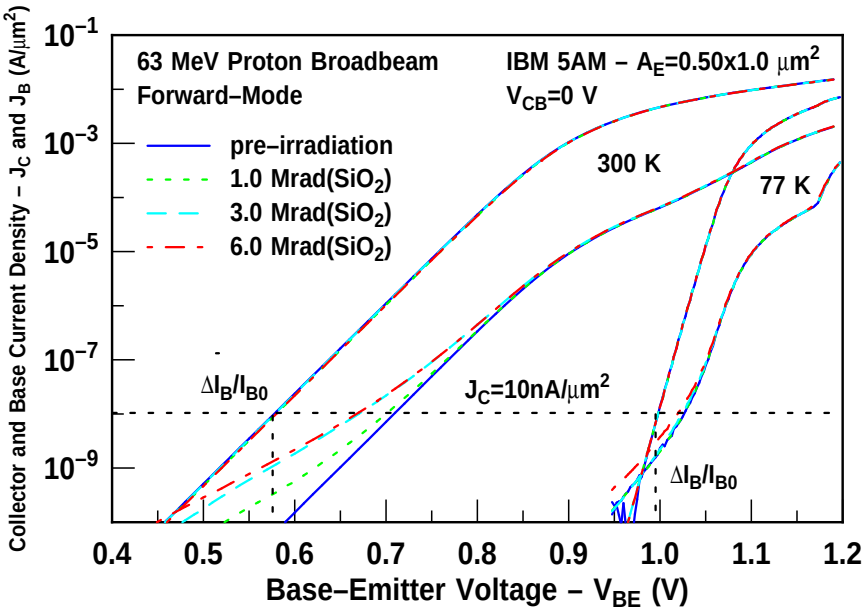

Figure 72: Forward-mode Gummel characteristics of 1$^{\mathrm{st}}$-generation HBTs irradiated with 63 MeV protons to a cumulative dose of 6 Mrad(SiO$_2$) at 77 K and 300 K.

In Figure 73, the forward-mode $\frac{\triangle I_B}{I_{B0}}\big|_{J_C=10\ \mathrm{nA}/\mu\mathrm{m}^2}$ is plotted as a function of dose for 1$^{\mathrm{st}}$- and 3$^{\mathrm{rd}}$-generation HBTs irradiated at 300 K and 77 K. In both technology platforms, there is more than an order of magnitude reduction in the forward mode $\frac{\triangle I_B}{I_{B0}}\big|_{J_C=10\ \mathrm{nA}/\mu\mathrm{m}^2}$ with cooling. A similar trend is observed in the inverse-mode $\frac{\triangle I_B}{I_{B0}}\big|_{J_C=10\ \mathrm{nA}/\mu\mathrm{m}^2}$. At 77 K, the unrecombined holes generated in the bulk SiO_2 remain relatively immobile for a considerably longer time than at 300 K. These unrecombined holes may remain in a self-trapped state, resulting in an increase in the positive SiO_2 trapped charge and a decrease in the CTRW-dependent Si/SiO_2 interface trap density. Therefore, for a lower interface trap density the radiation-induced ΔJ_B is reduced.

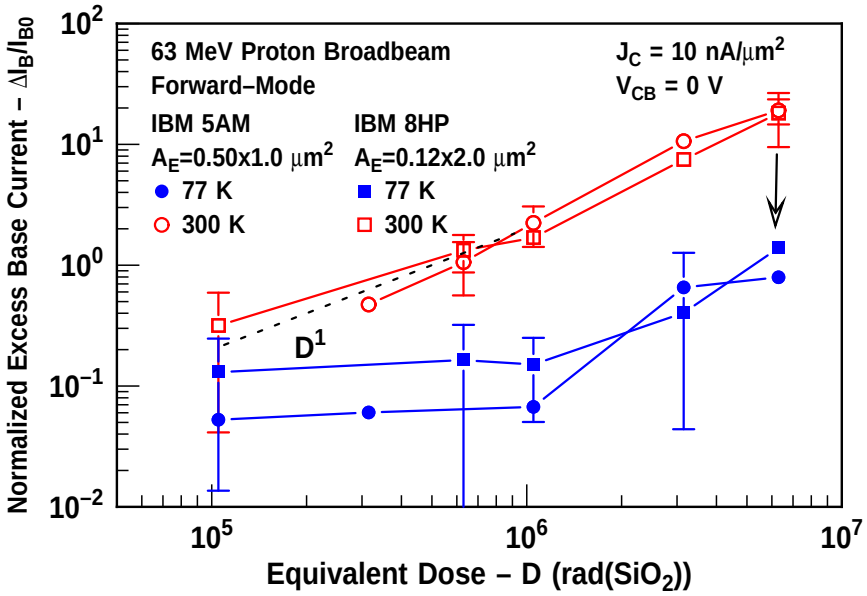

Figure 73: Forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}\big|_{J_C=10\ \mathrm{nA}/\mu\mathrm{m}^2}$ vs. 63 MeV proton dose for 1$^{\mathrm{st}}$- and 3$^{\mathrm{rd}}$-generation HBTs at irradiated at 300 K and 77 K.

6.3 Proton-Induced SEU Mechanisms

Energetic protons are known to degrade transistor performance via atomic displacement and ionization, both of which may be observed as shifts in either the threshold voltage (ΔV_{TH}) of a MOSFET [344] or the excess base current (ΔI_B) in a BJT [345]. In addition to these effects, the interaction of protons with the Si lattice, via both elastic and inelastic collisions, results in the creation of secondary particles. If these secondary particles have sufficient energy and range, then they are capable of inducing SEEs in logic and memory circuits [346][347].

Accurate predictions of the on-orbit event rate for space-based electronic components are vital for efficient system design and mission planning [348]. These rate predictions are routinely derived as the product of the orbit-dependent rate coefficient and the SEU figure of merit (SEU FOM), in units of upsets/bit/day [349]. The value of this rate coefficient is determined by the mission lifetime, local radiation fields, and ambient temperature. In a heavy-ion broadbeam environment, the SEU FOM is a function of the saturated error-event cross section ($\sigma_{EE\infty}$) and the threshold LET (L_{th}), while in a proton broadbeam environment, the limiting proton cross section (σ_{PL}) determines the SEU FOM [349]. Heavy-ion

broadbeam irradiation is typically performed using a variety of ions at different angles of incidence to simulate the orbital environment and generate the characteristic σ_{EE} vs. LET curve, from which the SEU FOM can be calculated. To date, heavy-ion broadbeam irradiation of HBT digital logic has only been performed at 300 K [330]-[332]. In this chapter, experimental results confirming an increase in the SEU response of HBT digital logic operating at cryogenic temperatures in a medium-energy proton broadbeam environment are presented.

6.4 Experiment Details

6.4.1 16-Bit Shift Registers

SEU phenomena in HBT digital logic are investigated using 16-bit shift registers composed of D-type flip-flops in addition to input, output, and clock buffers, as shown in Figure 74. The flip-flop components in these registers are implemented using the same CML architecture described in Chapter 5 and were fabricated in the 3rd-generation technology platform [233]. Both single-striped transistors, which are configured in a "CBE" layout with an A_E of 0.12×0.52 μm^2, and multiple-striped transistors, which are configured in a "CBEBC" layout with an A_E of 0.12×2.50 μm^2, are implemented in these registers. When compared to the multiple-striped "CBEBC" configuration, the "CBE" configuration has a smaller enclosed-DT area, which translates into a reduction in the substrate-to-sub-collector junction area and collector-collected charge [350].

The impact of circuit-level RHBD techniques on the proton-induced SEU response was evaluated by comparing shift registers designed using either the low-power standard master-slave (LP Std M/S) latch or the dual-interleaved (DI) latch, which are illustrated in Figures 59 and 61, respectively. The flip-flops in the LP Std M/S shift register were designed using the larger CBEBC-configured HBTs while those in the DI shift register were designed using the smaller CBE-configured HBTs. The input and clock buffers were identical for both registers and were designed using a gated-feedback cell (GFC) hardening approach [351], while the output buffers were designed using unhardened CML-based logic gates.

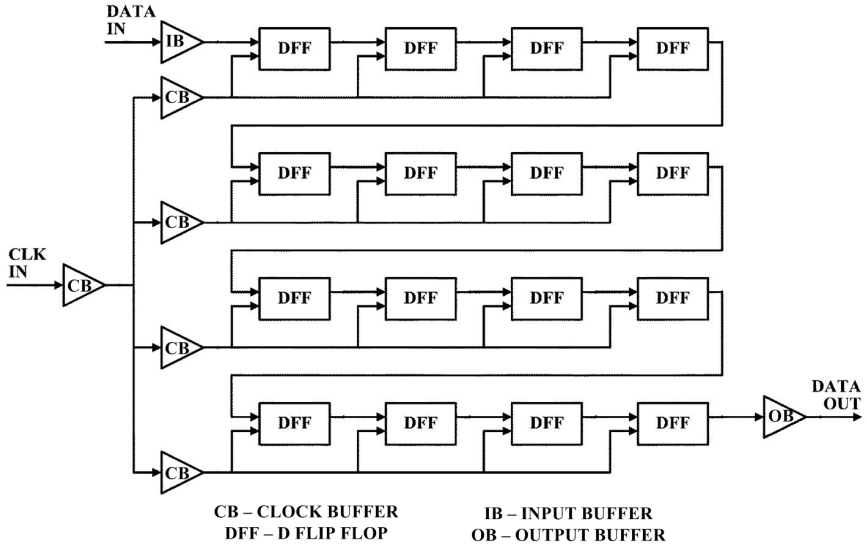

Figure 74: Generic top-level schematic of a 16-bit shift register.

Both shift registers are configured to operate on negative CML logic and use a 0 to -0.3 V peak-to-peak data swing in addition to ground (0 V) and power (V_{EE}=-4 V) supply rails. The area and power consumption of these shift registers are given in Table 7.

Table 7: Area and power consumption of the LP Std M/S and DI shift registers.

Architecture	Flip-Flop		16-bit Shift Register	
	A_E (μm^2)	I_{TAIL} (mA)	Area (mm^2)	Power (W)
LP Std M/S	0.12×2.50	60	1.4×2.2	0.23
DI [340]	0.12×0.52	130	1.4×2.2	0.58

6.4.2 Proton and Heavy-Ion Broadbeam Irradiation

The same experimental setup was used for proton and heavy-ion broadbeam irradiation. Three die of each shift register were packaged into separate custom-designed test fixtures capable of reliable high-speed operation at cryogenic temperatures. An image of these fixtures at the TAMU [217] beam line is shown in Figure 75. Proton broadbeam irradiation at 63 MeV was again performed at the CNL facility [203][204]. As was done for irradiation at the transistor level, circuit irradiation at 77 K was facilitated by immersing the high-speed test fixture in an EPS dewar filled with LN_2. Irradiations were performed in a manner that minimized the volume of LN_2 between the end of the beam line and the test fixture.

Again, as was done at the transistor level, an accurate temperature comparison was ensured by performing the irradiation at 300 K in the same EPS dewar, without any LN_2.

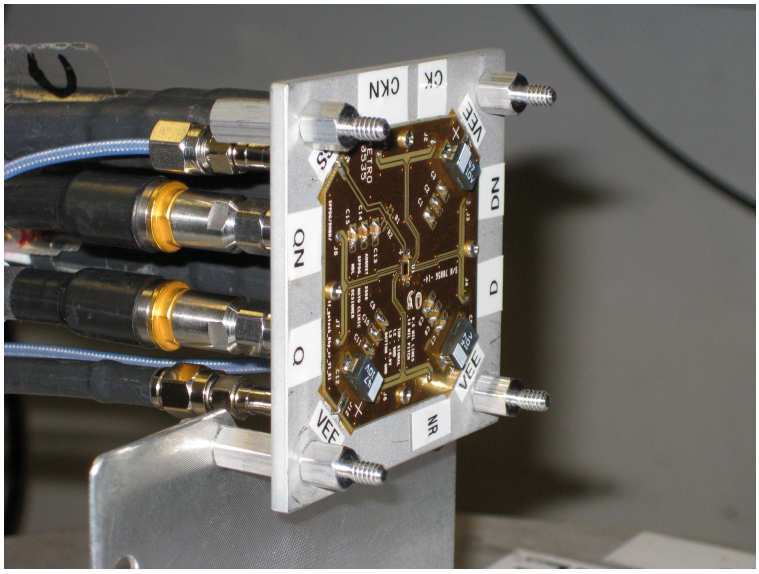

Figure 75: High-speed BER test fixture in the beam line at the TAMU cyclotron.

Heavy-ion broadbeam irradiation was performed at the TAMU facility [217] using 15 MeV/amu ^{20}Ne, ^{40}Ar, ^{84}Kr, and ^{129}Xe ions impingent on the shift registers at angles of incidence (θ) ranging from 0° to 60°. Nevertheless, comparisons of the proton- and heavy-ion-induced SEU response are facilitated using only the data generated by normally-incident heavy ions. The details of both radiation facilities are provided in Section 2.3.

BER testing was implemented using a 2^7-1 PRS that was generated by an Anritsu MP1763C pulse-pattern generator, and error detection and capture were facilitated via an Anritsu MP1764C 12.5 GHz BERT analyzer. The experimental setup is illustrated in Figure 76. A custom-built LabVIEW program was used to manage the GPIB control of all equipment, control error capture, and facilitate real-time analysis. Prior to beam insertion, the PRS voltage and phase thresholds required for error-free operation in each register were determined at both 300 K and 77 K for data rates ranging from 50 Mbit/s to 4 Gbit/s.

To have good BER statistics, a large number ($\ggg$100) of error-events is required, which means that the shift registers are typically exposed to a high proton fluence (1×10^{12} cm^{-2}). Therefore, the impact of atomic displacement and ionization on the SEU response of these

registers should be taken into account. The results from high-temperature broadbeam irradiation of commercial SRAMs from a variety of vendors indicated that total-dose degradation may indeed impact the SEU response of CMOS technology platforms [352]. In this chapter, these total-dose effects are accounted for by exposing multiple test fixtures on separate accelerator test trips with different temperature-cycling sequences. To be sure, it should be noted that the TID tolerance of these SiGe HBTs is significantly higher than that of the MOSFETs fabricated in the same technology node [353].

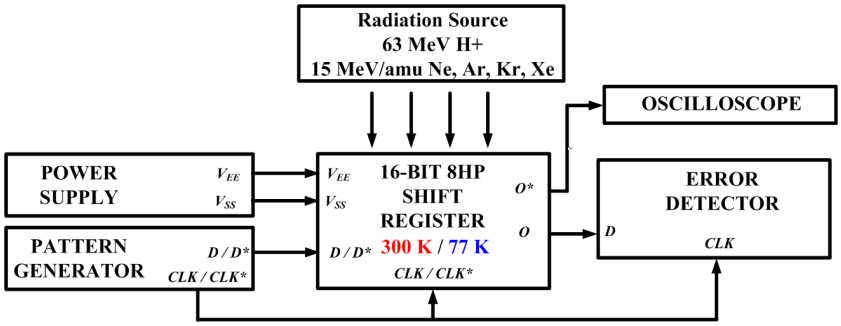

Figure 76: Variable-temperature BER test setup for proton and heavy-ion broadbeam irradiation.

6.5 Proton- and Heavy-Ion-Induced Cross Sections

The SEU response or "upset rate" of a shift register is quantified using the device cross section (σ). For 63 MeV protons, the device cross section (σ_P) can be expressed in terms of the proton energy (E_P), upset threshold (A), and limiting cross section (σ_{PL}) as [349]

$$\sigma_P = \sigma_{PL}\left[1 - \exp\left(-0.18 \times Y^{\,0.5}\right)\right]^4, \tag{98}$$

where

$$Y = \left(\frac{18}{A}\right)^{0.5}(E_P - A)\,. \tag{99}$$

During measurement, σ_P is calculated by simply dividing the number of errors recorded by the incremental particle fluence.

In this chapter, both the total number of error events (EE) and the total number of incorrect bits (BE) are used to analyze the upset rate. An error event refers to the complete PRS sequence that is captured once the input and output data streams fail to match,

and incorrect bits are collected for the duration of each run, regardless of the number of error events. Therefore, there are two different device cross sections that can be defined, which in the case of protons, are designated as $\sigma_{P(EE)}$ and $\sigma_{P(BE)}$. $\sigma_{P(EE)}$ is the proton-induced error-event cross section, which is obtained by normalizing the total number of error events to the incremental proton fluence, whereas $\sigma_{P(BE)}$ is the proton-induced bit-error cross section, which is obtained by normalizing the total number of incorrect bits to the incremental proton fluence. In a similar fashion, the heavy-ion-induced error-event $(\sigma_{HI(EE)})$ and bit-error $(\sigma_{HI(BE)})$ cross sections can be defined for heavy-ion broadbeam irradiation.

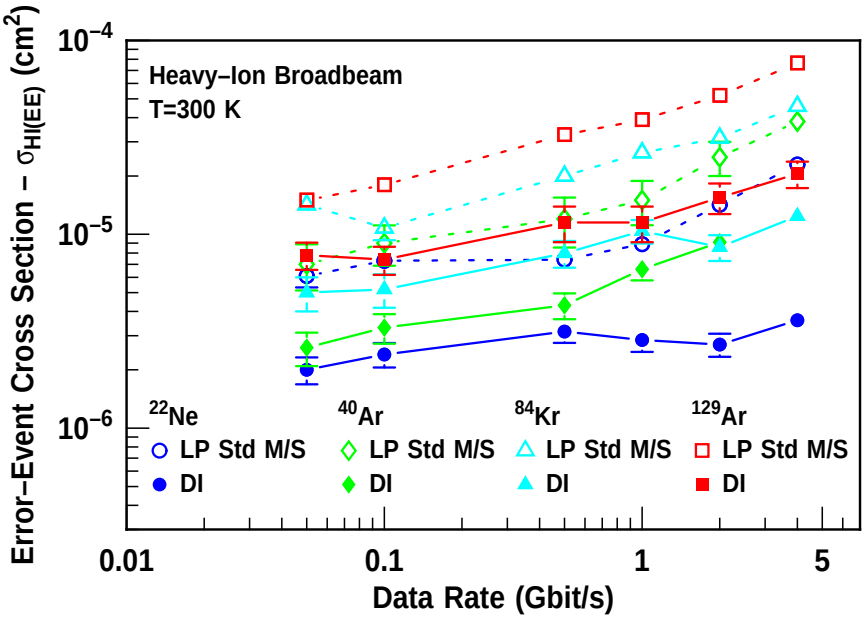

Figure 77: $\sigma_{HI(EE)}$ vs. data rate for the low-power standard master-slave and dual-interleaved shift registers irradiated with ^{22}Ne, ^{40}Ar, ^{84}Kr, and ^{129}Xe ions.

In Figure 77, $\sigma_{HI(EE)}$ is plotted as a function of data rate for 15 MeV/amu ^{22}Ne, ^{40}Ar, ^{84}Kr, and ^{129}Xe broadbeam irradiation of the LP Std M/S and DI shift registers. The error bars in Figure 77 (and all other cross section plots in this chapter) indicate one standard deviation bound on the data. Poisson statistics are invoked, and the standard deviation is calculated as the square-root of the number of error events (or bit errors) normalized to the incremental fluence. Heavy ions, which have large LETs, generate more e-h pairs, thereby increasing the transistor-level collector-collected charge and the number of error

events for a constant fluence and data rate. As the data rate is increased, the radiation-induced transient current and voltage waveforms span a greater number of clock cycles and increase the number of incorrect bits recorded at a constant LET and data rate. Finally, the implementation of latch-level redundancy in the DI shift register results in a 78% reduction in $\sigma_{HI(EE)}$ for ^{129}Xe broadbeam irradiation at a data rate of 4 Gbit/s.

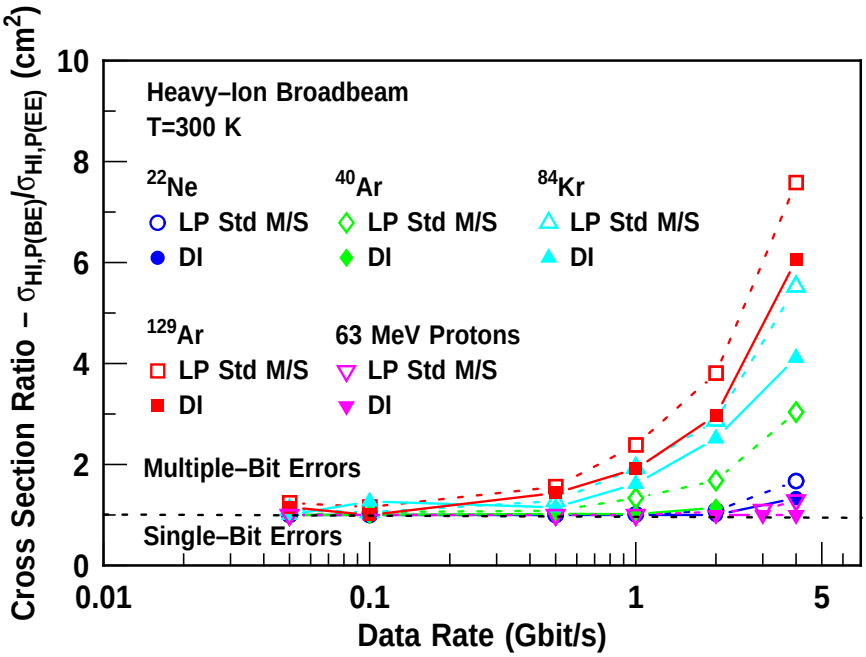

Figure 78: $\frac{\sigma_{HI,P(BE)}}{\sigma_{HI,P(EE)}}$ vs. data rate for the low-power standard master-slave and dual-interleaved shift registers irradiated with ^{22}Ne, ^{40}Ar, ^{84}Kr, ^{129}Xe ions, and 63 MeV protons.

The ratio of the cross section calculated from the number of bit errors to the cross section calculated from the number of error events $\left(\frac{\sigma_{HI,P(BE)}}{\sigma_{HI,P(EE)}}\right)$, which is heavily influenced by the error composition, is plotted as a function of data rate in Figure 78. If $\frac{\sigma_{HI,P(BE)}}{\sigma_{HI,P(EE)}}$=1, then single-bit errors dominate the upset rate since the number of error events is equal to the actual number of incorrect bits. Conversely, if $\frac{\sigma_{\mathrm{HI,P(BE)}}}{\sigma_{\mathrm{HI,P(EE)}}} \ggg 1$, then multiple-bit errors factor heavily into the overall upset rate. As shown in Figure 78, the proton-induced upsets in both the LP Std M/S and DI shift registers are dominated by single-bit errors up to a data rate of 4 Gbit/s.

Conversely, as the data rate and heavy-ion LET are increased, multiple-bit errors dominate the heavy-ion-induced upset rate. As illustrated in Figure 79, $\sigma_{P(EE)}$ is several orders

of magnitude lower than $\sigma_{HI(EE)}$ for both the LP-Std M/S and DI shift registers. To be sure, $\sigma_{P(EE)}$ and $\sigma_{P(BE)}$ are both lower than $\sigma_{HI(EE)}$ and $\sigma_{HI(BE)}$ because of the relatively low energy-dependent interaction probability for proton-Si reactions, as compared to the higher interaction probabilities and charge yield for the reactions of high-LET heavy ions with Si [349][354][355]. In addition, the partial decoupling of transistors in the storage cell of the DI latch results in over an order of magnitude reduction in $\sigma_{P(EE)}$ at 300 K. It should also be noted that no errors are observed for the DI shift register at data rates below 2 Gbit/s, whereas errors are observed for the LP Std M/S register at data rates down to 50 Mbit/s.

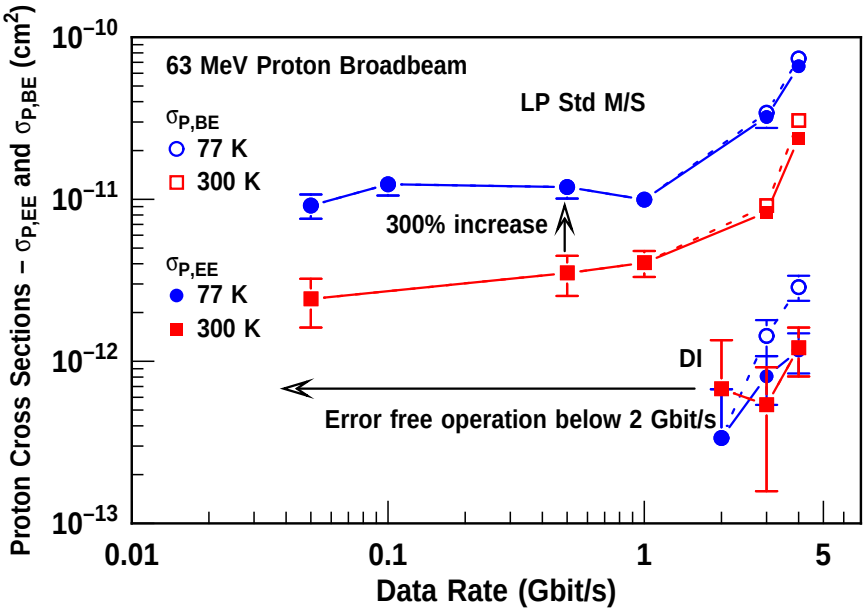

Figure 79: $\sigma_{P(BE)}$ and $\sigma_{P(EE)}$ vs. data rate for the low-power standard master-slave and dual-interleaved shift registers irradiated with 63 MeV protons at 300 K and 77 K.

Most importantly, in the case of the LP Std M/S shift register, $\sigma_{P(EE)}$ increases by over 300% as the temperature is cooled from 300 K to 77 K. Conversely, for the DI shift register, there is no noticeable change in $\sigma_{P(EE)}$ with cooling. These results clearly demonstrate an increase in the proton-induced upset rate at cryogenic temperatures and also indicate that the circuit-level RHBD techniques show promise for SEU mitigation in a low-temperature heavy-ion broadbeam environment.

6.6 Error Signature Analysis

Error events were detected by first comparing the input and output PRS using an XOR gate and captured by logging the entire bit stream for processing according to the methodology described in Section 5.2. As described in Chapter 5, the average BIE, SB%, and the percentage of 1→0 transitions are used as the primary figures of merit in comparing the upset rates of both latch architectures as a function of heavy-ion species and ambient temperature. The average BIE and SB% are plotted as a function of data rate in Figures 80 and 81(a), respectively. Both plots indicate that proton-induced upsets are dominated by single-bit errors up to 4 Gbit/s and are in agreement with the observed variation in $\frac{\sigma_{P(BE)}}{\sigma_{P(EE)}}$ as a function of data rate, which is illustrated in Figure 78. Moreover, single-bit errors dominate the proton-induced upsets at both 77 K and 300 K. Conversely, the average BIE for ^{84}Kr broadbeam irradiation rises steadily from one to ten, which corresponds to the reduction in the ^{84}Kr-induced SB% shown in Figure 81(a) and confirms the presence of multiple-bit errors in the heavy-ion-induced upset rate.

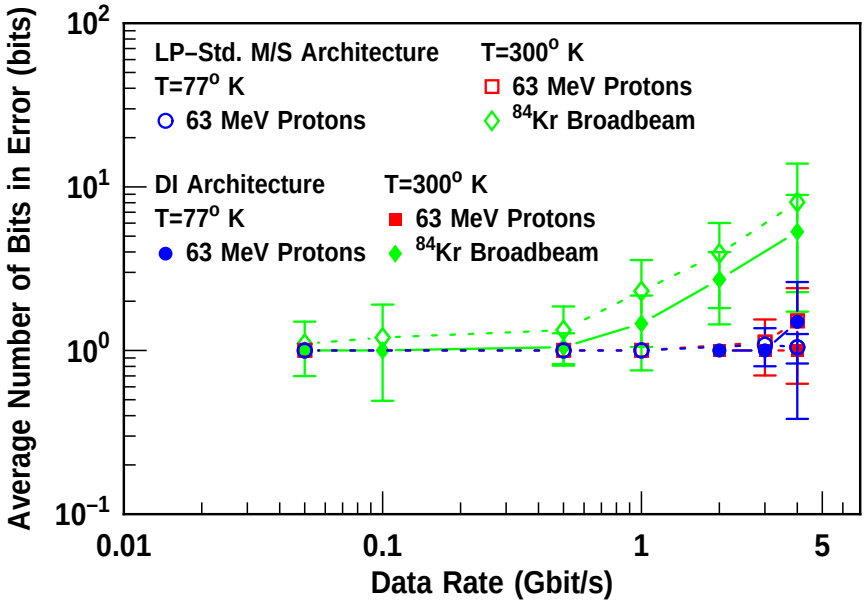

Figure 80: Average BIE vs. data rate for the low-power standard master-slave and dual-interleaved shift registers irradiated with ^{84}Kr ions at 300 K and 63 MeV protons at 300 K and 77 K.

As was demonstrated in Chapter 5, single-photon pulsed laser irradiation of both the local and root clock buffers in these shift registers results in an equivalent percentage of 1→0 and 0→1 transitions. This behavior is in contrast to the "flatten to 1" and "flatten to 0" errors that are observed for pulsed laser irradiation of transistors in the pass cell of the master latch in the LP Std M/S register (Q_1 and Q_2 in Figure 59). However, in both the proton and heavy-ion broadbeam environment, the percentage of 1→0 transitions is equal to the percentage of 0→1 transitions across the range of data rates tested. This result is illustrated in Figure 81(b) and suggests that both the proton- and heavy-ion-induced upset rates are dominated by ion strikes to the clock buffers.

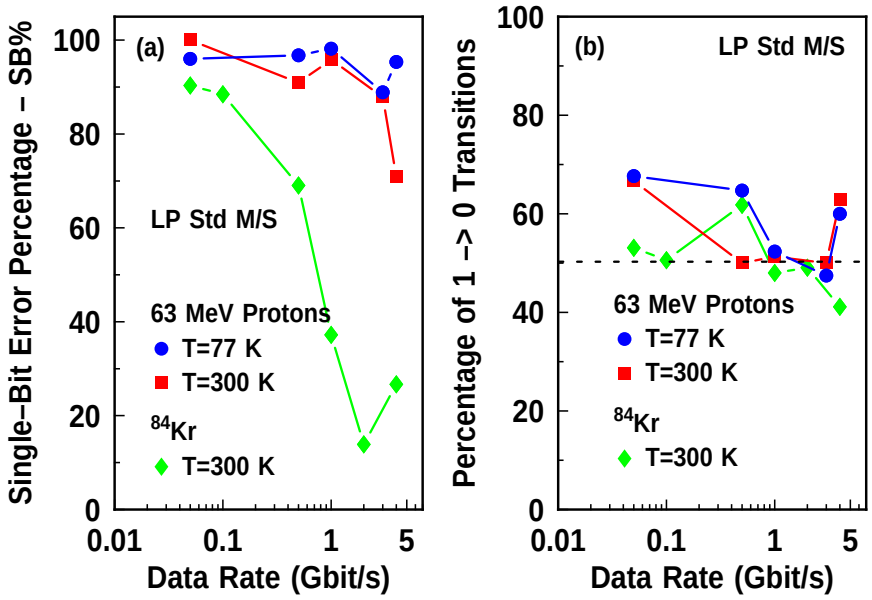

Figure 81: (a) SB% and (b) percentage of 1→0 transitions vs. data rate for the low-power standard master-slave shift register irradiated with ^{84}Kr ions at 300 K and 63 MeV protons at 300 K and 77 K.

6.7 2-D TCAD Charge Collection Simulations

Several theoretical models have been proposed to account for the increase in the electron (μ_e) and hole (μ_h) mobilities at cryogenic temperatures. These models typically invoke the effects of phonon scattering resulting from lattice vibrations [356], ionized-impurity scattering in heavily-doped regions, carrier-to-carrier scattering resulting from the high carrier density immediately after the passage of a heavy ion, and impurity scattering occurring at low temperatures and doping levels [356]. From an experimental perspective, a 500% increase in both μ_e and μ_h has been observed in Si when the ambient temeperature was reduced from 300 K to 77 K [357]. That observation is consistent with the increase in the charge-collection volume and resultant upset rate at low temperature. Furthermore, in additional investigations it has been concluded that the electron (τ_e) and hole (τ_h) lifetimes both decrease as the ambient temperature is lowered [358]. Clearly, these reductions in τ_e and τ_h are counterintuitive to the enhanced in $\sigma_{P(EE)}$ and $\sigma_{P(BE)}$ reported in this chapter.

To determine whether it is the carrier mobility or the carrier lifetime that causes the increased upset rate at cryogenic temperatures, calibrated 2-D TCAD simulations were performed on a 1st-generation HBT diode. The doping-dependent Masetti mobility model and Scharfetter recombination lifetime equations were implemented in a drift-diffusion solver with carrier-to-carrier scattering turned on. Non-physical changes in μ_e, μ_h, τ_e, and τ_h were used to mimic the effects of a reduction in the ambient temperature. Ion strikes were simulated using the parameters of a low-energy proton with an LET of 10 MeV·cm^2/g, and three sets of simulations were performed at the corresponding "temperature." In the first set of simulations, μ_e and μ_h were modified in the device parameter file, and all other parameters were held constant. In the second set, τ_e and τ_h were modified, and all other parameters were held constant. Finally, in the third set, μ_e, μ_h, τ_e, and τ_h were all modified. Even though these simulations were run at at 300 K, all parameter modifications emulate the cryogenic-temperature behavior based on previously reported data [359].

In the simulated HBT diode, the substrate terminal was used as the anode and the collector as the cathode. The anode and cathode voltages were set to 0 V and 3.3 V, respectively. Starting from nominal (300 K) values of τ_e=10 μs and τ_h=3 μs, when τ_e

and τ_h were increased by as much as 150X, there was no change in the transient-current waveform. Conversely, starting from nominal values of μ_e=1417 cm^2/V·s and μ_h=470 cm^2/V·s, when μ_e and μ_h were increased by just 30X, a significant enhancement in the peak collector current ($I_{C,peak}$) was observed. This result is illustrated in Figure 82(a). As shown in Figure 82(b), a 200% increase in the collector-collected charge, which is derived as the time integral of I_C, is observed approximately 0.1 μs after the ion strike. These results suggest that the enhancement in the proton-induced upset rate at cryogenic temperatures is dominated by mobility enhancement.

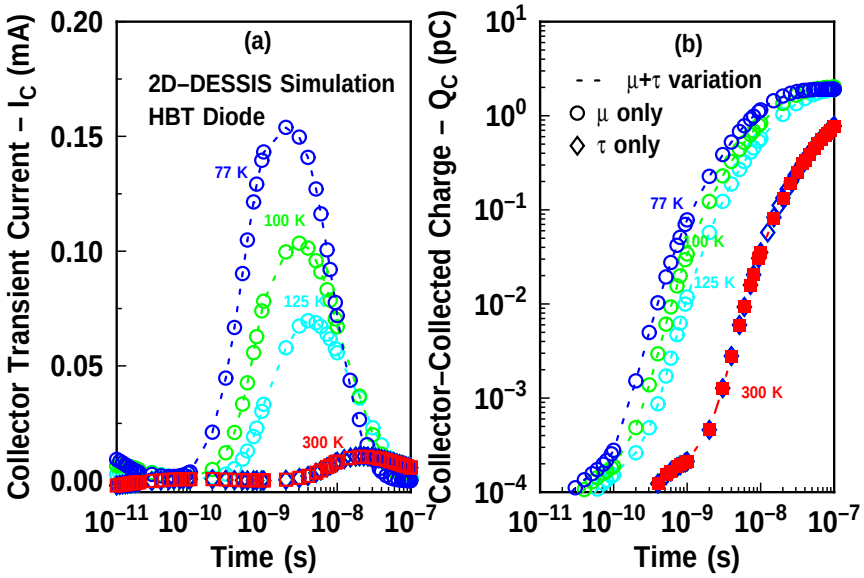

Figure 82: 2-D TCAD simulations of the low-temperature heavy-ion-induced (a) I_C and (b) Q_C of an HBT diode obtained via μ_e and τ_e modification.

A similar approach was used to simulate the enhancement in the proton-induced collector-collected charge for 1st-generation HBT at 77 K. In this simulation, μ_e was increased by an order of magnitude from its nominal (300 K) value. The nominal value of μ_e was chosen by calibrating the simulated charge-collection profiles to the heavy-ion microbeam data presented in [360]. The collector-collected charge (Q_C) is plotted as a function of the lateral position across the transistor (x_C) in Figure 83. A 10X increase in μ_e yields a 100% increase in Q_C for heavy ions impingent outside of the DT, which is consistent with the increased proton-induced upset rate at cryogenic temperatures.

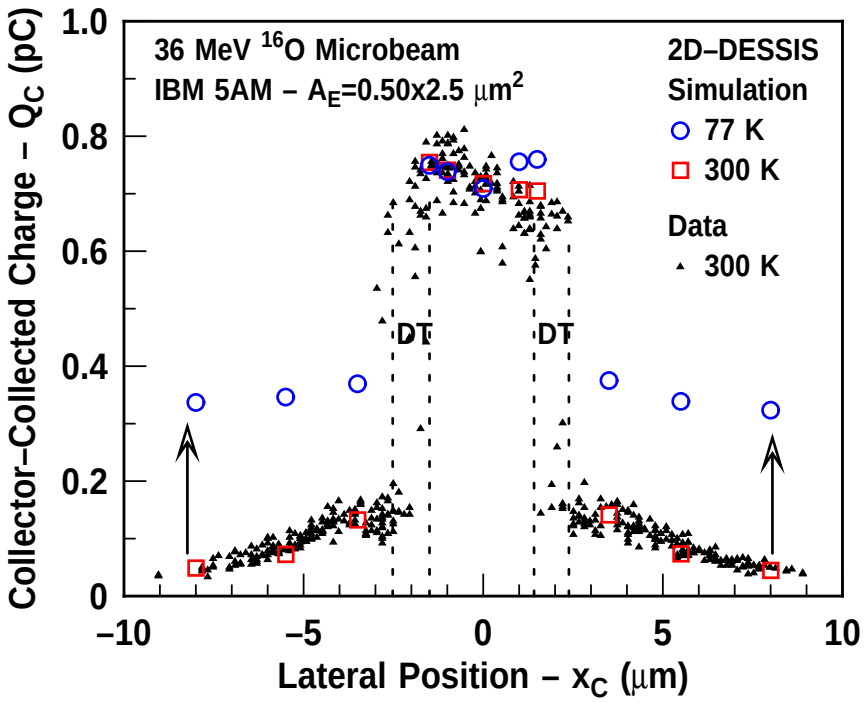

Figure 83: 2-D TCAD simulations of the low-temperature Q_C of a 1st-generation HBT obtained via μ_e modification.

6.8 Conclusion

An experimental validation of enhanced SEEs at cryogenic temperatures has been presented using medium-energy proton irradiation of HBT digital logic in LN_2. At room temperature, the proton-induced error-event and bit-error cross sections are several orders of magnitude less than the corresponding heavy-ion-induced cross sections. Moreover, the proton-induced upsets are dominated by single-bit errors up to a data rate of 4 Gbit/s, regardless of the ambient temperature. Most importantly, as the temperature is reduced from 300 K to 77 K, the proton-induced error-event and bit-error cross sections both increase by over 300%. 2-D TCAD simulations indicate that these effects are driven primarily by temperature-induced increases in the carrier mobility, despite simultaneous reductions in the carrier lifetime. Additionally, circuit-level RHBD techniques are proven to be successful in the mitigation of the enhanced proton-induced upset rate at 77 K. These results strongly suggest the need for further investigation into the heavy-ion-induced SEE response as a function of temperature.

CHAPTER 7

TRANSISTOR-LEVEL LAYOUT-BASED RHBD TECHNIQUES

7.1 Introduction

The effects of atomic displacement, ionization and SEEs on 1st- and 3rd-generation HBTs and HBT digital logic have been described in Chapters 3-6. The results presented thus far indicate that although SiGe HBTs are tolerant to multi-Mrad(SiO_2) ionization levels, HBT digital logic remains extremely sensitive to SEEs. SEE mitigation in HBT digital logic continues to be a major research area, with recent heavy-ion broadbeam irradiation results demonstrating limiting error-event and bit-error cross sections, which are indicative or error-free operation, at ion LETs well above 50 MeV·cm^2/mg for 16-bit shift registers fabricated in the 3rd-generation technology platform [350]. This milestone was achieved by encapsulating a dual-interleaved shift register in a TMR architecture along with voting-at-end (VAE) circuitry [342][361]. Although successful, this TMR-based mitigation technique results in a significant area and power penalty. In this chapter, a transistor-level layout-based approach for SEE mitigation in HBT digital logic is presented.

After a heavy ion traverses through the Si bulk and substrate potential-modulation effects have subsided, unrecombined carriers are efficiently swept away by any pre-existing electric fields. In many microelectronic devices these electric fields are associated with reverse-biased pn-junctions, and the field-induced carrier transport is a drift-dominated processes [59][362]. For the npn SiGe HBTs investigated in this chapter, the *pn* junction of interest is the reverse-biased substrate-to-sub-collector junction. Based on 3-D TCAD charge-collection simulations of these HBTs, collector and emitter terminals have been identified as sinks for electrons, and the base and substrate terminals have been identified as sinks for holes. The fractional charge collected by each terminal depends on the load

impedance, terminal bias, substrate doping, and heavy-ion range [341][363]. The terminal-collected charge results in voltage perturbations, which cause the experimentally observed broadbeam circuit response in [331][364].

In the first section of this chapter, the transistor-level layout-based RHBD approach is presented and its impact on the total-dose tolerance and transistor performance is be addressed. This approach involves the implementation of an additional low-impedance sink for electrons within the transistor. This low-impedance sink is realized by the inclusion of an alternate reverse-biased *pn* junction designed to shunt electron charge away from the substrate-to-sub-collector junction. This alternate *pn* junction is referred to as the "n-ring." The inclusion of the n-ring affects neither the *dc* nor the ac performance of the transistor, and the multi-Mrad(SiO_2) TID tolerance of the transistor is not compromised.

In the second section, the results from 36 MeV ^{16}O microbeam irradiation are used to investigate the impact of heavy-ion track location, angle of incidence, n-ring placement, and n-ring bias on the collector-collected charge. The findings indicate that charge shunting through the n-ring causes reductions of up to 90% in the collector-collected charge for heavy ions impingent outside the DT. Conversely, if the heavy ion is impingent inside the DT, then the reduction in the collector-collected charge is only 18%.

In the third section, 3-D NanoTCAD ion-strike simulations are used to verify the experimental observations, as well as to shed insight into the underlying physical mechanisms. Finally, the chapter is concluded with a discussion of the implications for RHBD approaches to SEE mitigation in HBT digital logic.

7.2 Transistor-Level Implementation

7.2.1 Layout Variations

Several variations of the n-ring have been incorporated into 3rd-generation SiGe HBTs [233]. These transistors all feature an A_E of 0.12×3.0 μm^2 and are implemented in a single-striped CBE configuration. The top-down and cross section schematics of six implementations of the n-ring in these SiGe HBTs are illustrated in Figure 84.

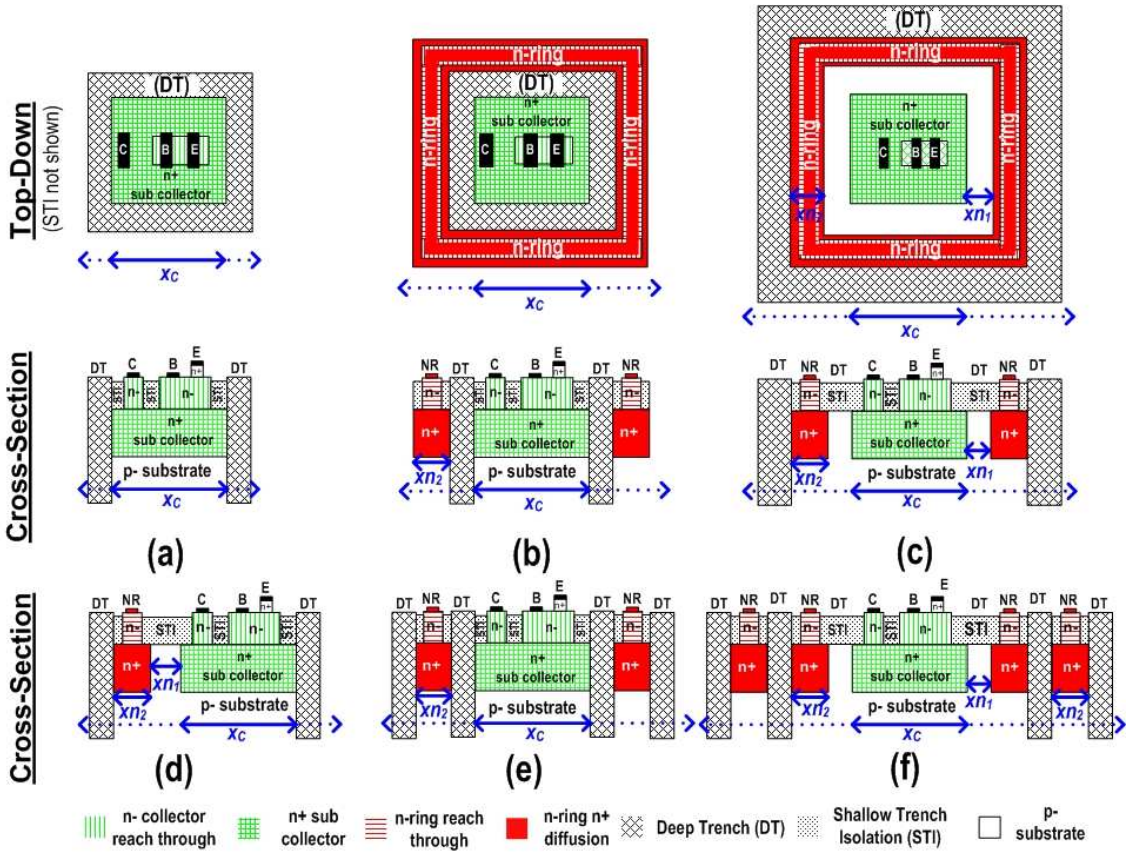

Figure 84: Top-down and cross section schematics of the transistor-level layout-based RHBD approach as applied to 3rd-generation HBTs including the (a) nominal-HBT, (b) external R-HBT, (c) internal R-HBT, (d) 1-sided R-HBT, (e) 1NR-2DT R-HBT, and (f) 2NR-2DT R-HBT.

In Figure 84, the lateral position across the transistor is denoted as x_C, the width of the n-ring is denoted as x_{n2}, and the spacing between the n-ring and the sub-collector is denoted as x_{n1}. An unhardened HBT, hereafter referred to as the *nominal*-HBT, was chosen as the "control" and is illustrated in Figure 84(a). The n-ring can be implemented either inside or outside of the DT. The *external* R-HBT features an n-ring implemented on the outside of the DT, as shown in Figure 84(b). Conversely, the *internal* R-HBT features an n-ring implemented on the inside of the DT, as shown in Figure 84(c). Additional RHBD variants can be derived by selectively changing the values of x_{n1}, x_{n2}, x_C, and the location of the DT. To address the area penalty inherent to the internal R-HBT, an RHBD variant with an internal "n-stripe," which is located on one side of the DT, was also fabricated. This

variant is known as the *1-sided* R-HBT and is shown in Figure 84(d). Finally, the impact of the DT location relative to the n-ring is addressed by the fabrication of RHBD variants with multiple DT and n-ring regions. These variants are known as the *1NR-2DT* R-HBT and the *2NR-2DT* R-HBT and are shown in Figures 84(e) and (f), respectively. The prefix "1NR-2DT" is used to indicate the presence of one n-ring and two trenches, while the prefix "2NR-2DT" is used to indicate the presence of two n-rings and two trenches.

In all RHBD variants, the width of the n-ring is 2 μm (x_{n2}=2 μm) and the n-ring-to-sub-collector spacing varies between 3 and 8 μm ($3 \leqslant x_{n1} \leqslant 8$ μm). In the 3$^{\text{rd}}$-generation technology platform, if $x_{n1} \leqslant 2.5$ μm, then out-diffusion of the n-ring and sub-collector doping profiles during fabrication results in those two regions being electrically shorted together, rendering the transistor inoperable. Clearly, several variations in the internal R-HBT are realized for different values of x_{n1}, and to delineate amongst these, the specific internal R-HBT under investigation will be identified by using the value of x_{n1} as a prefix.

7.2.2 *dc* and *ac* Performance Characteristics

The forward-mode Gummel and f_T vs. J_C characteristics are illustrated in Figures 85(a) and (b), respectively.

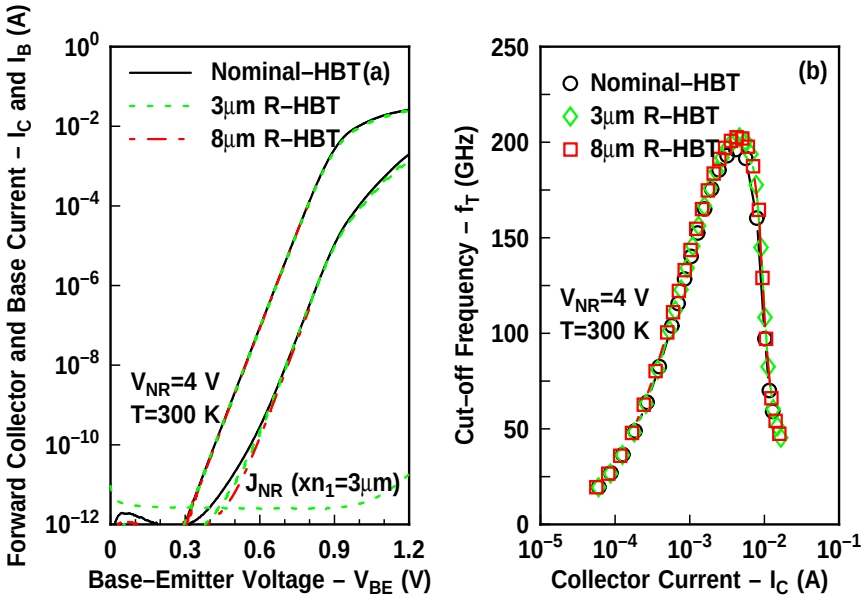

Figure 85: (a) Forward-mode Gummel characteristics and (b) f_T vs. J_C of the 8μm-internal R-HBT.

The inclusion of the n-ring in these 3rd-generation HBTs degrades neither the *dc* nor the *ac* performance of the transistor, regardless of any variations in the n-ring bias (V_{NR}) and spacing (x_{n1}). Furthermore, the reverse-bias current density of the substrate-to-n-ring junction (J_{NR}) is well below 1pA for the entire voltage sweep in the Gummel characteristic, as shown in Figure 85(a).

The inclusion of the n-ring, whether internal or external, also creates a parasitic npn BJT between the n-ring (n), substrate (p), and sub-collector (n). The n-ring current (I_{NR}) is plotted as a function of V_{NR} for the internal R-HBT in Figure 86(a). When all other transistor terminals are grounded (V_{SX}=V_C=V_B=V_E=0 V), the substrate-to-n-ring breakdown voltage (BV_{SXNR}) is 25 V for x_{n1}=8 μm. As x_{n1} is reduced, BV_{SXNR} decreases significantly to 12.5 V at x_{n1}=5 μm and to 9 V at x_{n1}=3 μm. In addition, the substrate-to-sub-collector junction breakdown voltage (BV_{SXC}) is illustrated in Figure 86(b). At V_{NR}=0 V, BV_{SXC} is 10 V for x_{n1}=5 μm, and as V_{NR} is increased, BV_{SXC} is reduced to 8 V at V_{NR}=2 V and to 6 V at V_{NR}=4 V. If x_{n1} is reduced in addition to increasing V_{NR}, then further reductions in BV_{SXC} are observed.

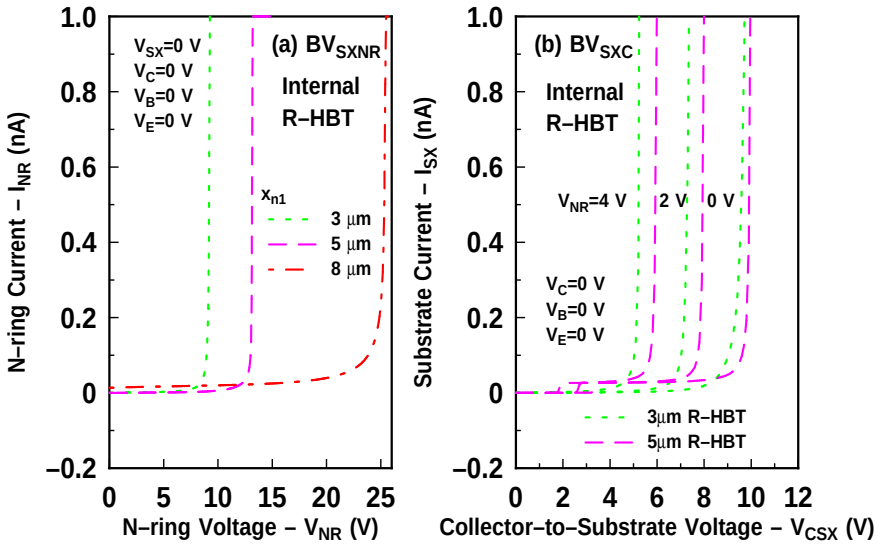

Figure 86: (a) I_{NR} vs. V_{NR} and (b) I_{SX} vs. V_{CSX} of the 3μm-, 6μm-, and 8μm-internal R-HBTs.

7.2.3 Proton-Induced Ionization Effects

The 8 μm-internal R-HBT was irradiated with 63.3 MeV protons at the CNL facility [203][204], which has been described in Section 2.3.3. Several *dc* test structures of each RHBD variant were packaged into 28-pin DIPs using the procedure described in Chapter 3, and irradiations were performed with all transistor terminals grounded. The pre- and post-irradiation Gummel characteristics were measured using the Agilent 4155 SPA.

As shown in Figure 87, there are no significant differences between the proton-induced $\frac{\triangle I_B}{I_{B0}}$ of the nominal-HBT and the 8 μm-internal R-HBT after irradiation to a cumulative dose of 3 Mrad(SiO_2). This result is observed in both the forward and inverse mode, and follows from the fact that the inclusion of the n-ring does not alter the physical location of the BE spacer and STI Si/SiO_2 interfaces. As demonstrated in Chapters 3 and 4, it is at these interfaces where the radiation-induced interface trap density, which determines the excess base current, is expected to be highest [239]. Furthermore, both the forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}$ are not affected by changes in V_{NR}.

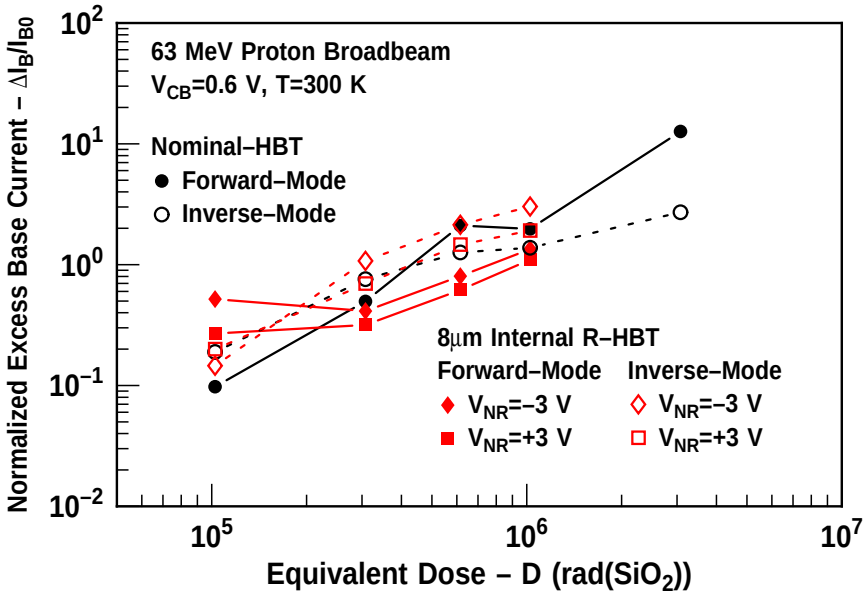

Figure 87: Forward- and inverse-mode $\frac{\triangle I_B}{I_{B0}}$ vs. 63 MeV proton dose for the nominal-HBT and 8μm-internal R-HBT.

7.3 Heavy-Ion Microbeam Analysis

7.3.1 Experiment Details

Heavy-ion microbeam irradiation was performed at the SNL facility [218]-[220], which was described in Section 2.3.3. ^{16}O ions with an energy of 36 MeV, a range of 25.5 μm in Si, a surface LET of 5.2 MeV·cm^2/mg, a Bragg peak of 7.5 MeV·cm^2/mg, and a 1-μm spot size were stepped across a 100×100 μm^2 field encompassing the active area of the transistor. The heavy-ion-induced charge collected on the collector, base, emitter, substrate, and n-ring terminals was monitored for ^{16}O ions impingent at two angles of incidence (θ=0° and 15°). Prior to microbeam irradiation, a non-destructive fluorine-based RIE was used to selectively remove several microns of inter-metal dielectric above the transistor, thereby increasing the amount of charge deposited into the substrate underlying the active area.

7.3.2 Impact of N-ring Layout and Spacing

The data obtained from heavy-ion microbeam irradiation is composed of the microbeam coordinates in the x-y plane and the the corresponding charge collected on each terminal. This 3-D charge-collection map was reduced by taking a 1-μm slice along the y-axis around the peak value of the collector-collected charge (Q_C). These position-dependent values of Q_C were then projected onto the x-axis and plotted as a function of the lateral position across the transistor. A slice width of 1 μm was chosen to avoid sampling too many events originating outside the DT while ensuring that a representative charge-collection profile was captured.

The peak value of Q_C and the path integral of Q_C along x_C ($Q_{C,INT}$) are used as the figures of merit for comparing the SEE mitigation capability of the various transistor-level layout-based RHBD variants. $Q_{C,INT}$ can be written as

$$Q_{C,INT} = \int_a^b Q_C(x_C)dx_C, \tag{100}$$

where a and b are the limits of integration, which extend outside the DT on the left and right, respectively, to a point where the collector-collected charge vanishes. The peak value of Q_C is representative of the collector-collected charge from a heavy ion impingent at the

center of the emitter contact, while $Q_{C,INT}$ is representative of the cumulative collector-collected charge resulting from multiple heavy ions impingent across the entire length of the 1 μm slice. Q_C is plotted as a function of x_C for the nominal-HBT, 8μm-internal R-HBT, 3μm-internal R-HBT, and the external R-HBT in Figure 88. In all cases, the ^{16}O ions are normally incident on the transistor, and in the case of the RHBD variants, V_{NR} is set to 4 V.

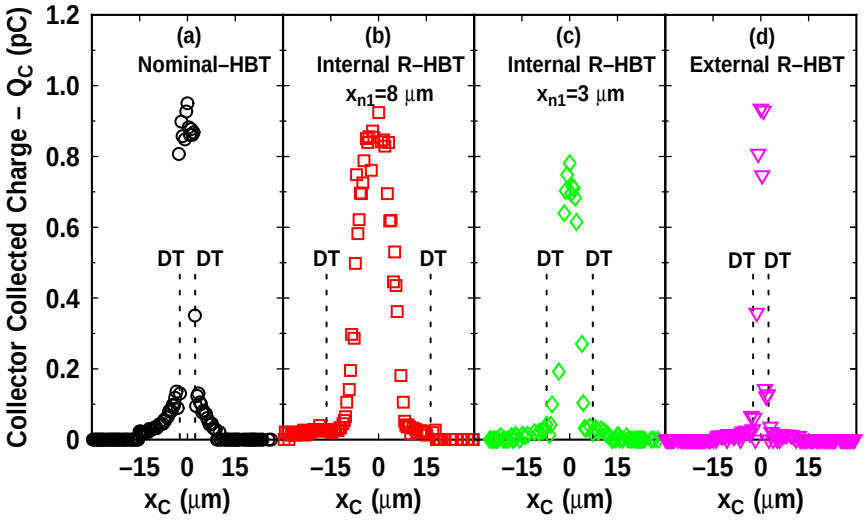

Figure 88: Q_C vs. x_C for the (a) nominal-HBT, (b) 8μm-internal R-HBT, (c) 3μm-internal R-HBT, and (d) external R-HBT all irradiated with ^{16}O ions.

^{16}O ions deposit 26 MeV of energy and generate 1.1 pC of charge in Si. A previous charge-collection study of 2nd-generation HBTs [232] using this ion source yielded a peak Q_C of approximately 1.0 pC, which represents a 90% charge-collection efficiency [332]. A heavy ion that is normally incident on the center of the emitter contact deposits the largest amount of charge in the substrate and corresponds to the peak Q_C values illustrated in Figure 88. ^{16}O ions incident on the nominal-HBT yield a peak Q_C of 0.95 pC inside the DT and 0.1 pC outside the DT. In the case of the internal R-HBT, there is no change in peak Q_C for x_{n1}=8 μm; however, as x_{n1} is scaled down to 3 μm, a slight reduction is observed. Conversely, ^{16}O ions incident inside the DT of the external R-HBT yield a peak Q_C that is almost identical to that of the nominal-HBT, and interestingly, there is significant suppression in Q_C for ^{16}O ions impingent outside the DT of the external R-HBT

. These results suggest that although the external R-HBT offers no immunity for heavy ions impingent inside the DT, significant mitigation is provided for those impingent outside the DT.

7.3.3 Impact of N-ring Voltage

The value of V_{NR} at a fixed-V_{SX} determines the reverse-bias voltage on the substrate-to-n-ring junction, which determines the depletion width, electric field, electrostatic potential, and the spatial volume for drift-dominated charge collection by this *pn* junction. The path-integrated collected charge, which was defined for the collector terminal in (100), can also be defined for the n-ring ($Q_{NR,INT}$) and substrate ($Q_{SX,INT}$) terminals. $Q_{C,INT}$, $Q_{NR,INT}$, and $Q_{SX,INT}$ are plotted as a function of x_C for the 3 μm-internal R-HBT and the external R-HBT in Figure 89.

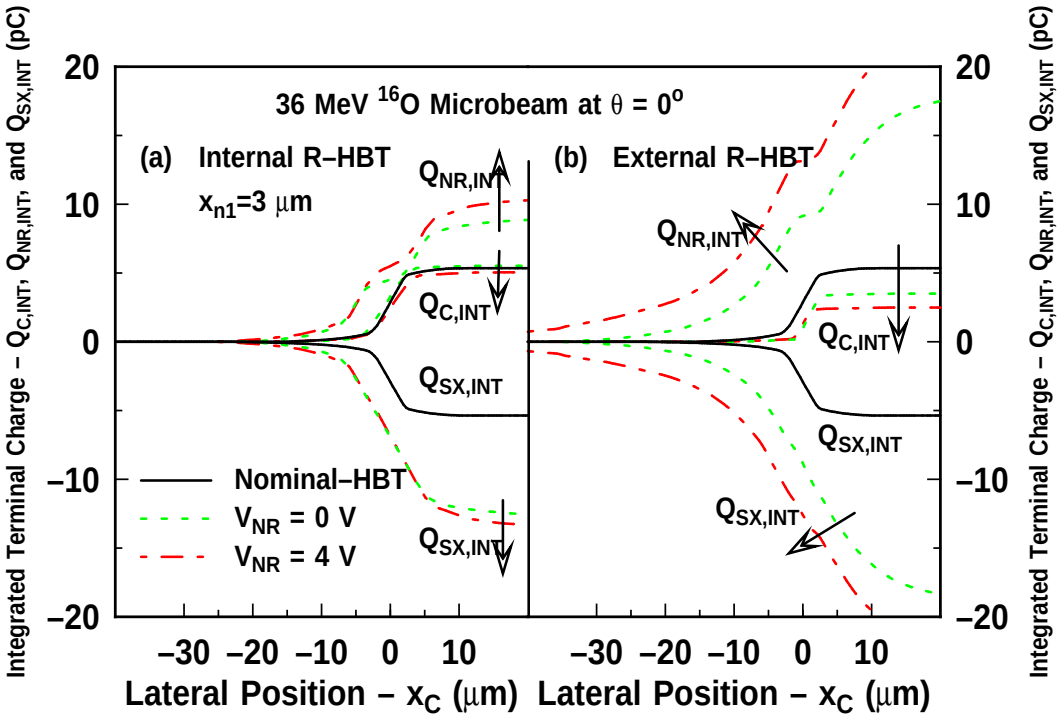

Figure 89: $Q_{C,INT}$,$Q_{NR,INT}$, and $Q_{SX,INT}$ vs. x_C for the (a) 3μm-internal and (b) external R-HBTs all irradiated with ^{16}O ions at θ=0°.

As expected from prior investigations [332], charge collection on the base (Q_B) and emitter (Q_E) terminals is negligible. Therefore, since Q_B and Q_E are relatively small, electron

collection is dominated by the collector and n-ring terminals, and hole collection is dominated by the substrate. This hypothesis is supported by the fact that $Q_{C,INT}+Q_{NR,INT}\approx Q_{SX,INT}$ for both the internal and external R-HBTs at V_{NR} values of 0 V and 4 V.

Q_C is plotted as a function of x_C at V_{NR}=0 V and 4 V for both the 3 μm-internal R-HBT and the external R-HBT in Figure 90. Increasing V_{NR} yields a noticeable increase in both $Q_{NR,INT}$ and $Q_{SX,INT}$ along with a slight decrease in $Q_{C,INT}$. The external n-ring collects approximately 2X more electrons than the internal n-ring and is more sensitive to changes in V_{NR}. However, although the external n-ring collects 2X more electrons than the internal n-ring, it offers no mitigation against heavy ions impingent inside the DT. Conversely, when biased at V_{NR}=4 V, the internal n-ring yields an 18% reduction in peak Q_C. Moreover, the changes in V_{NR} have very little effect on peak Q_C for both the internal and external R-HBTs.

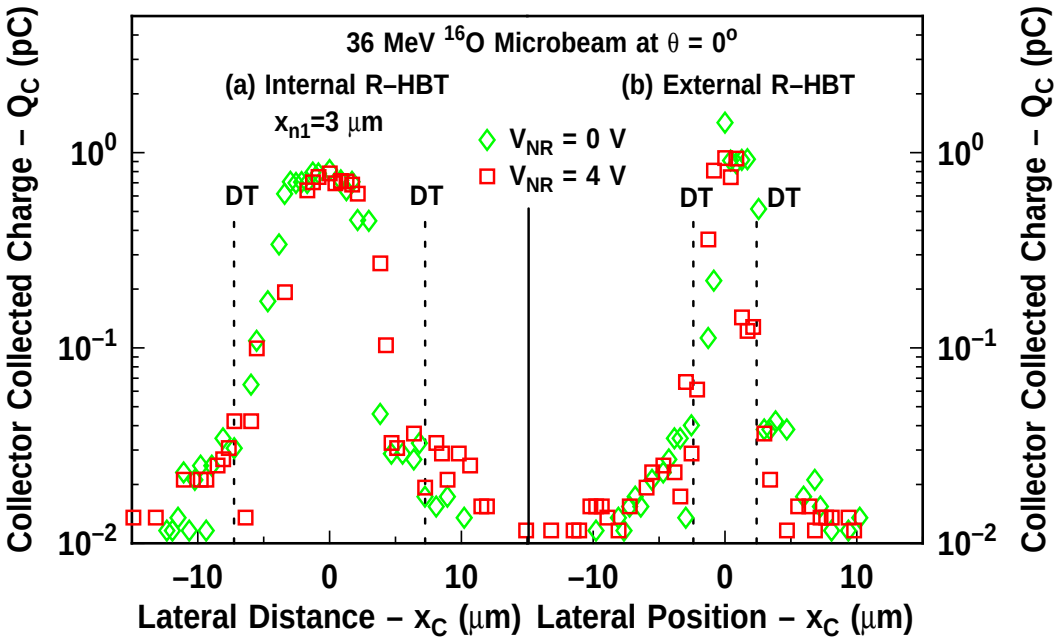

Figure 90: Q_C vs. x_C for the (a) 3μm-internal and (b) external R-HBTs all irradiated with ^{16}O ions at θ=0°.

7.3.4 Impact of Ion Location and Angle of Incidence

In addition to V_{NR}, the location of the incident ^{16}O ion relative to the DT and the value of θ at which the ion is impingent on the transistor can both impact the dependence

of Q_C on x_C. In Figure 91, Q_C is plotted as a function of x_C for both the 3 μm-internal R-HBT and the external R-HBT at V_{NR}=4 V and at θ=0° and 15°. ^{16}O ions impingent on the center of the emitter contact have the largest charge-deposition volume available to them, and unrecombined carriers are efficiently collected via both drift and funneling processes [362]. If the ions are impingent on the transistor at a location outside the DT, then the excess e-h pairs must first diffuse under the DT before they can be collected via drift, which results in a Q_C value that is at least an order of magnitude smaller than for ions impingent inside the DT. The external n-ring provides a reduction of up to 90% in Q_C for ^{16}O ions impingent outside the DT, while the internal n-ring provides no mitigation.

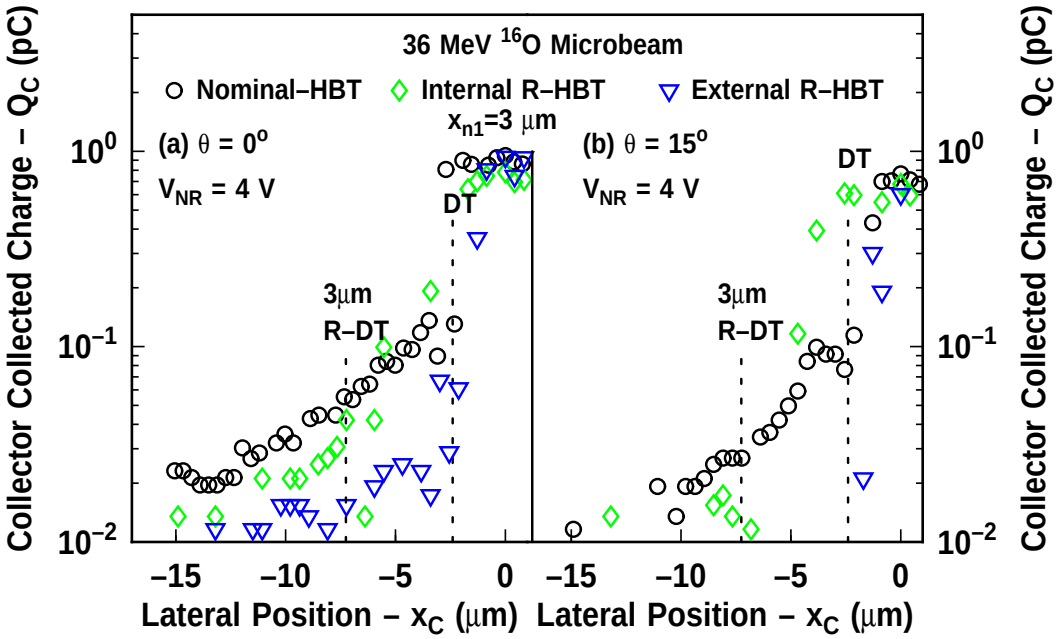

Figure 91: External-DT Q_C vs. x_C for the nominal-HBT, 3μm-internal and external R-HBTs all irradiated with ^{16}O ions at (a) θ=0° and (b) θ=15°.

As θ is increased from 0° to 15°, a 20% reduction in peak Q_C is observed for ^{16}O ions impingent inside the DT of the nominal-HBT, 3 μm-internal R-HBT, and external R-HBT. When θ is increased from 0° to 15°, there is an increasingly asymmetric component of Q_C for ions impingent outside the DT. Furthermore, at θ=15°, the external n-ring completely eliminates Q_C for ions impingent outside the DT, and $Q_{NR,INT}$ and $Q_{SX,INT}$ are also reduced, as illustrated in Figure 92.

The "effective LET" (L_{eff}) for heavy ions impingent on the transistor at θ can be written as

$$L_{eff} = \frac{L}{\cos(\theta)}, \tag{101}$$

where L is the LET at normal incidence. It should be noted that there have been several experimental results, based on CMOS SRAMs, that contradict the validity of this model [365]. In the case of these 3rd-generation HBTs, as θ is increased, the path length of ^{16}O ions in the BEOL material also increases, and the ^{16}O ion energy near the active are of the transistor is reduced. Additionally, perturbation of the ion track through the DT may also contribute to the observed reduction of internal-DT collection.

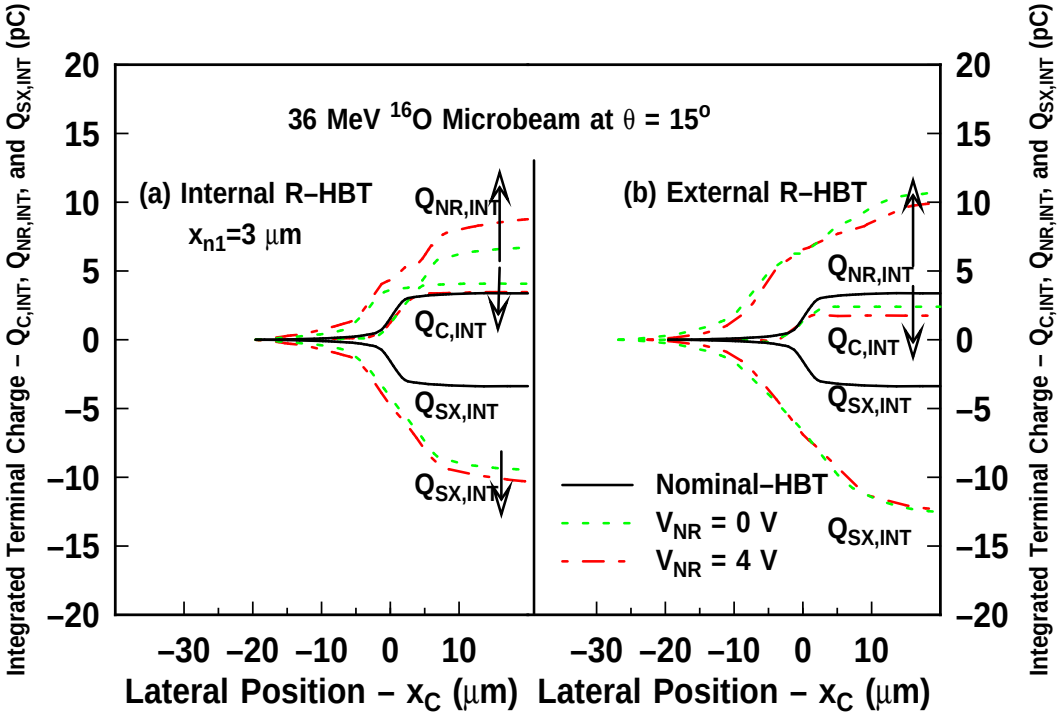

Figure 92: $Q_{C,INT}$,$Q_{NR,INT}$, and $Q_{SX,INT}$ vs. x_C for the (a) 3μm-internal and (b) external R-HBTs all irradiated with ^{16}O ions at θ=15°.

7.3.5 Impact of N-ring Area

One of the major disadvantages of the internal R-HBT is the increase in the enclosed deep-trench area (A_{DT}), which increases the drift-dominated charge collection volume relevant to the substrate-to-sub-collector junction. To reduce A_{DT}, the n-ring can be converted

into either a single or double "n-stripe," as illustrated in Figure 84(d). Although this transformation reduces A_{DT}, these RHBD variants now also suffer from a reduction in the total n-ring area (A_{NR}), and the resultant $Q_{NR,INT}$ is reduced by 90% when compared to the internal R-HBT, as shown in Figure 93(b) and (c). In this case, the substrate-to-sub-collector junction area is larger than the substrate-to n-ring-junction area, which suggests that the electric field associated with the sub-collector-to-substrate junction accounts for the majority of the drift-dominated charge collection and explains the increase in $Q_{C,INT}$ for these reduced-A_{DT} R-HBTs.

As demonstrated in the previous section, the utilization of the external n-ring yields the largest reduction in Q_C for ^{16}O ions impingent outside the DT. It should be noted that the substrate-to-n-ring junction of the external R-HBT is not bounded by the DT, which enables radiation-induced excess carriers to be efficiently collected in both the vertical and lateral direction.

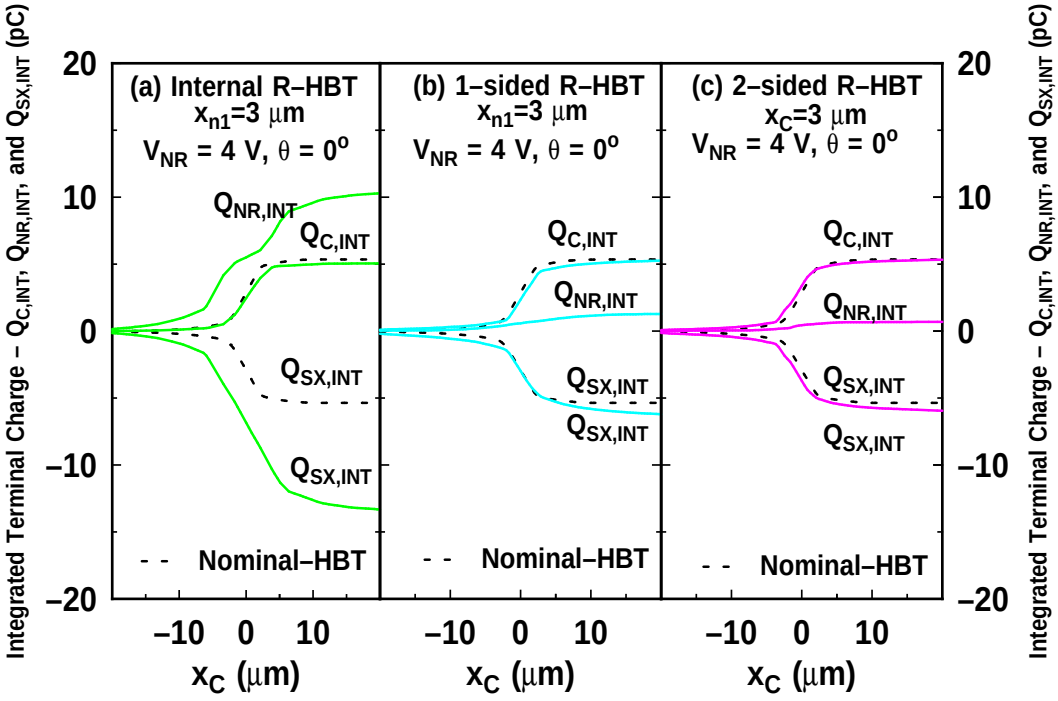

Figure 93: $Q_{C,INT}$,$Q_{NR,INT}$, and $Q_{SX,INT}$ vs. x_C at θ=0° for the (a) 3μm-internal R-HBT, (b) 3μm 1-sided R-HBT, and (c) 3μm 2-sided R-HBT all irradiated with ^{16}O ions.

The encapsulation of this external n-ring via the incorporation of a 2nd DT results in a 50% reduction in $Q_{NR,INT}$ since much of the drift-dominated n-ring collection in the

lateral direction is now eliminated, as shown in Figure 94(b). A schematic cross section of this RHBD variant, known as the 1NR-2DT R-HBT, is illustrated in Figure 84(e). The final RHBD variant under consideration is realized by combining the internal and external n-rings in the same transistor, thereby creating the 2NR-2DT R-HBT, as shown in Figure 84(f). In Figure 94(f), $Q_{NR,INT}$ is plotted as a function of x_C for the 2NR-2DT R-HBT and is observed to increase significantly along with a corresponding decrease in $Q_{C,INT}$. Although $Q_{C,INT}$ for the 2NR-2DT R-HBT is approximately equal to $Q_{C,INT}$ for the 3-μm internal R-HBT, there is an inherent 200% area penalty involved in choosing the 2NR-2DT R-HBT, which is clearly undesirable from a circuit-design perspective.

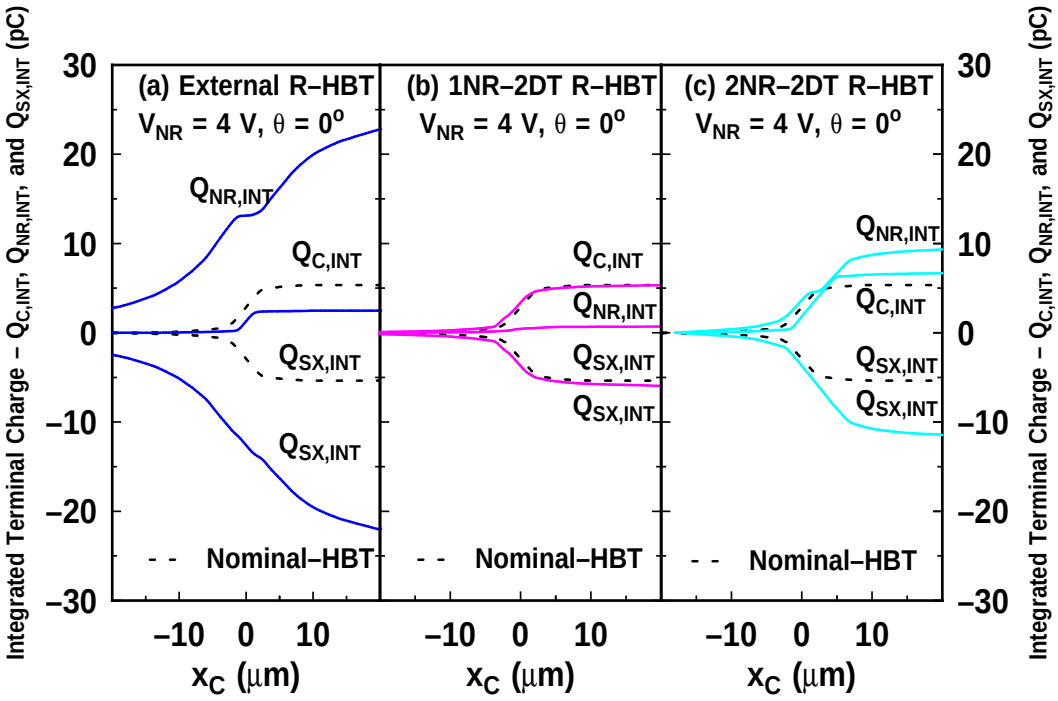

Figure 94: $Q_{C,INT}$,$Q_{NR,INT}$, and $Q_{SX,INT}$ vs. x_C at θ=0° for the (a) external R-HBT, (b) 1NR-2DT R-HBT, and (c) 2NR-2DT R-HBT all irradiated with ^{16}O ions.

7.3.6 Heavy-Ion Microbeam Charge Collection Summary

In Table 8, the ^{16}O-induced Q_C is summarized for all RHBD variants at normal incidence (θ=0°) and for selected RHBD variants at θ=15°. The ratio of the n-ring area to the enclosed-DT area $\left(\frac{A_{NR}}{A_{DT}}\right)$ heavily influences the value of Q_C. The peak Q_C and $Q_{C,INT}$ are plotted as a function of $\frac{A_{NR}}{A_{DT}}$ in Figures 95 and 96, respectively.

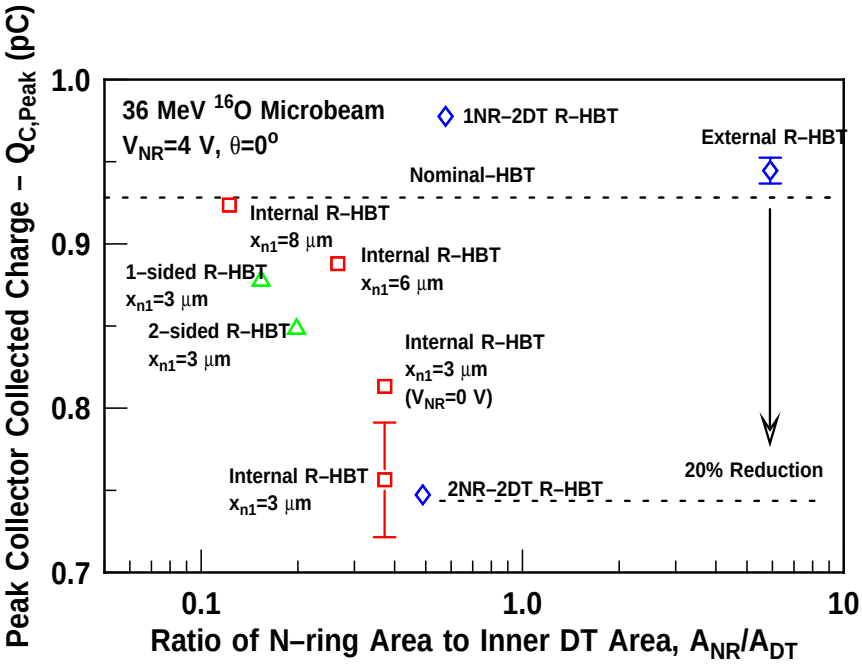

Figure 95: Peak Q_C vs. $\frac{A_{NR}}{A_{DT}}$ for all layout-based transistor-level RHBD variants all irradiated with ^{16}O ions.

In addition to the peak Q_C and $Q_{C,INT}$, the collector-collected charge for ^{16}O ions impingent on the substrate at 1 μm outside the DT is tabulated as $Q_C(DT+1)$.

Table 8: A_{NR} and A_{DT} for all RHBD devices compared to ^{16}O microbeam induced $Q_C(E)$, $Q_C(DT+1)$, and $Q_{C,INT}$ at θ=0^o and 15^o.

Transistor Type	θ	A_{DT} (μm^2)	A_{NR} (μm^2)	$Q_C(E)$ (pC)	$Q_C(DT+1)$ (pC)	$Q_{C,INT}$ (pC)
Nominal-HBT	0^o	11	NA	0.950	0.133	5.34
3 μm Internal R-HBT	0^o	172	29	0.781	0.017	3.16
6 μm Internal R-HBT	0^o	363	43	0.888	0.039	9.55
8 μm Internal R-HBT	0^o	972	54	0.924	0.027	11.63
External	0^o	11	59	0.935	0.012	2.48
1-sided	0^o	24	1.2	0.878	0.115	5.36
2-sided	0^o	37	2.4	0.845	0.102	5.36
1NR-2DT	0^o	69	16	0.978	0.021	6.68
2NR-2DT	0^o	326	68	0.749	0.020	5.33
Nominal	15^o	11	NA	0.766	0.051	3.38
3 μm Internal R-HBT	15^o	172	29	0.679	0	3.46
External	15^o	11	59	0.602	0	1.74

As previously demonstrated, the inclusion of the external n-ring results in a 90% reduction in Q_C for ^{16}O ions impingent outside the DT. This reduction in external-DT charge

collection is the driving force behind the 53% reduction in the overall $Q_{C,INT}$ for the external R-HBT and represents the largest mitigation offered out of all the RHBD variants tested. The addition of a 2nd DT on the outside of this structure, as shown in Figure 84(e), slightly reduces this advantage from 90% to 85%.

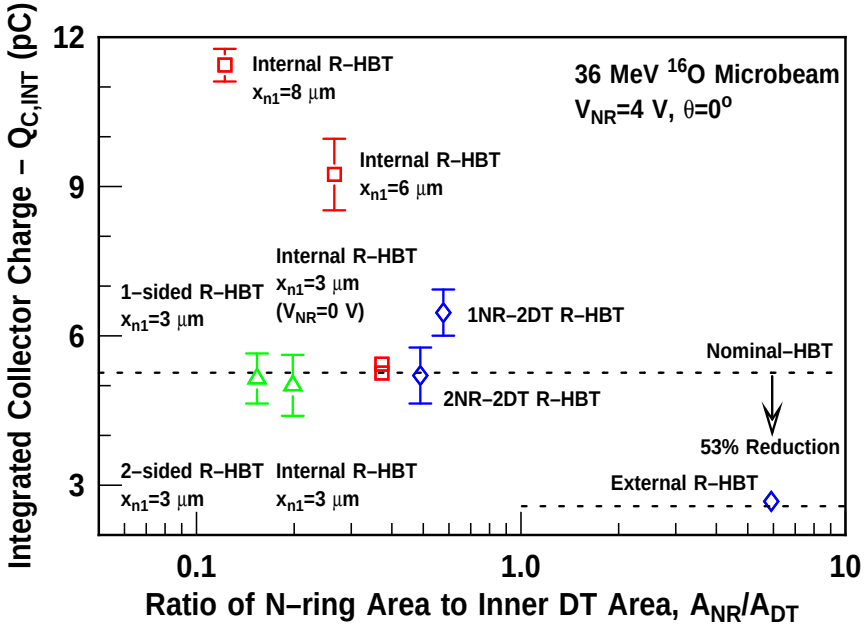

Figure 96: $Q_{C,INT}$ vs. $\frac{A_{NR}}{A_{DT}}$ for all layout-based transistor-level RHBD variants all irradiated with ^{16}O ions.

7.4 3-D TCAD Charge Collection Simulations

Charge-collection simulations were performed using the 3-D NanoTCAD simulation package [366], which has been previously used to simulate radiation effects on a range of modern IC technologies [367]-[369]. First, the layout information of each layer from the substrate through to the 1st-level metal was imported in GDS II format from Cadence into a meshing utility. Next, a solid-geometry model of the transistor, which measured 26×26×25 μm^3, was constructed using a binary-tree mesh. Localized mesh refinement was applied along the heavy-ion track and near the pn-junctions. To manage computation complexity, the BE spacer, STI, and DT oxides were not meshed. The simulated electron density 77 ps after an ^{16}O ion strike is illustrated in Figure 97.

Although a small mesh volume is desired for computational efficiency, the very nature of

an ion strike mandates that the mesh volume be large enough to capture the time-dependent variations in the excess carrier concentration following the strike. If the mesh volume is too small, then the reflective boundary conditions applied at the edges result in a non-physical "reflection" of the ion-strike-induced excess carriers. To reconcile these divergent requirements, a "wrapping layer" with an artificially-low carrier lifetime (τ_{WR}) of 50 ns was used to encase the entire substrate volume, and a standard carrier lifetime of 9 μs was used throughout the substrate. Secondary ion mass spectroscopy (SIMS) data was used to reproduce the doping profiles as a series of rectangular well regions with a constant dopant density enclosed by Gaussian-distributed tails along the edges.

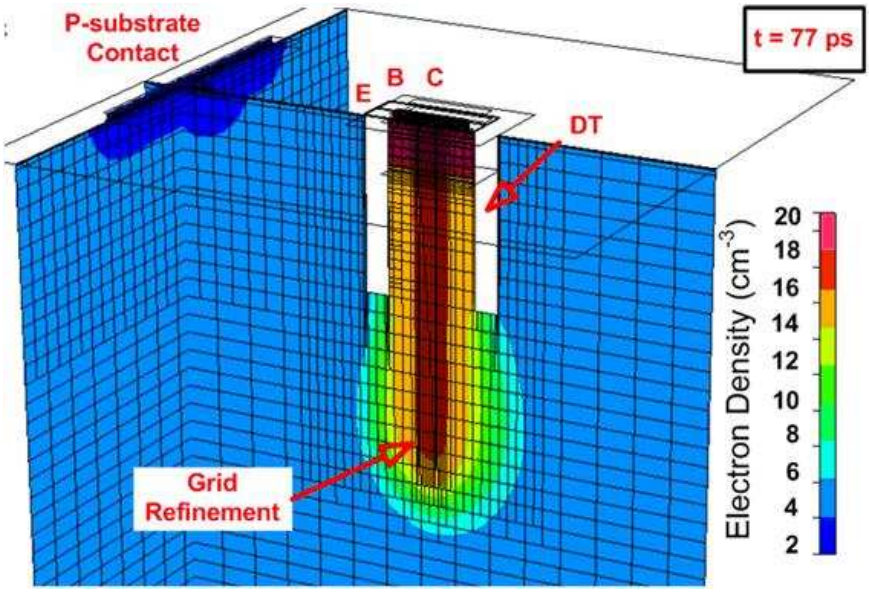

Figure 97: NanoTCAD 3-D simulation of the electron density 77 ps after a heavy-ion strike at the center of the emitter terminal.

Doping-dependent carrier lifetimes, SRH and Auger recombination, and mobility models that accounted for doping, electric fields, and carrier-to-carrier scattering were all implemented in the simulations, which were performed using a two-step approach. First, steady-state conditions were established by specifying the initial boundary and volume conditions. Next, an ion strike was simulated with the transistor initially configured in the steady-state condition derived in the first step. The incident ions were simulated at an LET of

7 MeV·cm^2/mg, which corresponds to the Bragg peak of the ^{16}O ions used in microbeam irradiation. An ion range of 13.72 μm was chosen to account for the 8 μm of dielectric material located over the transistor, and a Gaussian-distributed charge track was selected with a peak at 2 ps, a 1/e characteristic time scale of 0.25 ps, and a radius of 0.1 μm. To account for the impact atomic displacement and ionization on the collector-collected charge, an interface trap density of 5×10^{11} cm^{-2} was placed along the Si/SiO$_2$ interfaces of the BE spacer, STI, and DT. This value is typically used for studying total-dose effects in BJTs [370].

Ion strikes were also simulated for the external R-HBT and the 3-μm internal R-HBT. These models utilized similar parameters as for the nominal-HBT, with the exception that the lateral mesh area was extended from 26×26 μm^2 to 40×40 μm^2. The NanoTCAD package was used to solve the fundamental carrier-continuity and Poisson equations via the finite-volume numerical method, and post processing was performed using the CFD-View visualization package. A typical transient simulation covered up to 10 μs after the ion strike and took three hours on a 2.4 GHz Pentium PC.

The radiation-induced transient currents following an ^{16}O ion strike through the center of the emitter contact of the nominal-HBT are illustrated in Figure 98(a). I_C, I_B, I_E, and I_{SX} are used to denote the radiation-induced transient current on the collector, base, emitter, and substrate terminals, respectively. These current waveforms are composed of a prompt component, which lasts 5 to 10 ps after the waveform peaks, and a delayed component, which can persist for up to 2 ns after the ion strike. The prompt component is dominated by drift transport via the electric fields of the substrate-to-sub-collector and base-to-collector junction. Conversely, the delayed component is dominated by both carrier diffusion and drift transport via the electric field of the substrate-to-sub-collector junction. Prompt collection is observed on all terminals, but delayed collection is observed only on the collector and substrate. The delayed component accounts for the majority of the terminal-collected charge.

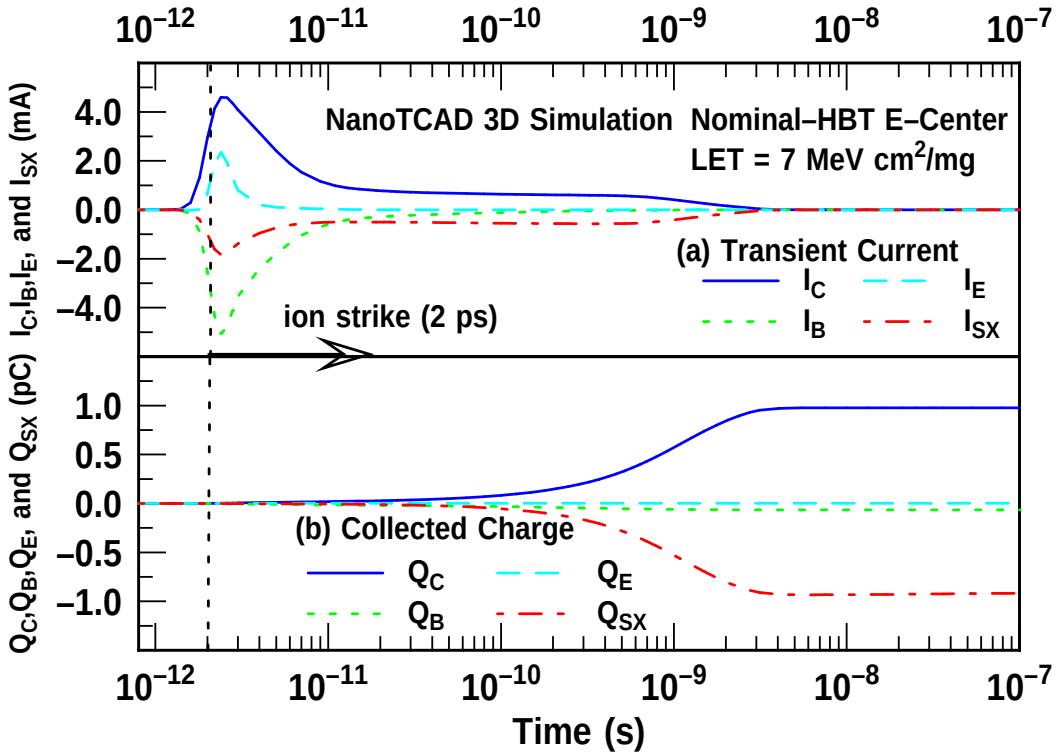

Figure 98: (a) I_C, I_B, I_E, and I_{SX}; (b) Q_C, Q_B, Q_E, and Q_{SX} for a 3-D TCAD simulation of ^{16}O ions impingent inside the DT of the nominal-HBT.

Q_C, Q_B, Q_E, and Q_{SX} are used to denote the radiation-induced charge that is collected on the collector, base, emitter, and substrate terminals. As shown in Figure 98(b), the collector and substrate terminals dominate the total charge collected since $Q_C \approx Q_{SX} \approx 1$ pC and $Q_E \approx Q_B \approx 0$ pC. These results are in reasonably good agreement with the DESSIS quasi-3-D TCAD simulations of ion strikes on 3rd-generation SiGe HBTs that was presented in [363][371].

Using the same parameters, ^{16}O ion strikes were also simulated outside the DT of the nominal-HBT, and the corresponding transient currents are illustrated in Figure 99(a). In this case there is no prompt component to the transient current on any terminal, and the delayed component is observed only on the collector and substrate terminals. The peak of the delayed component is observed 4 ns after the ion strike and is three orders of magnitude smaller than the prompt component. This suppression results in only 0.07 pC of charge being collected after 100 ns, as shown in Figure 99(b).

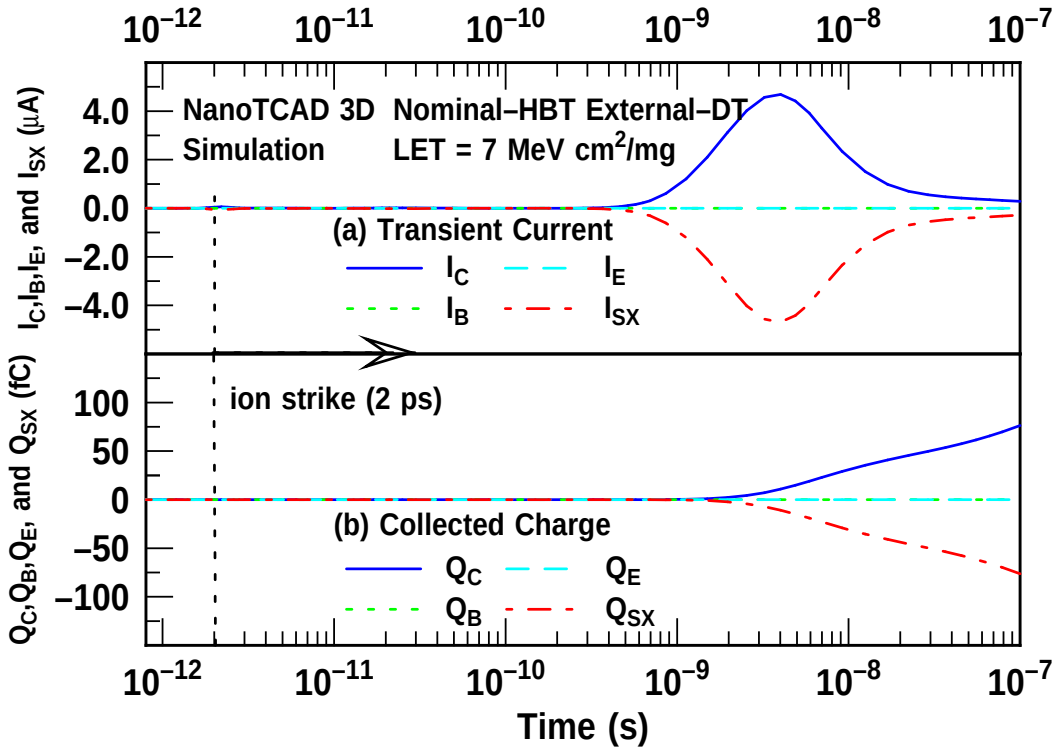

Figure 99: (a) I_C, I_B, I_E, and I_{SX}; and (b) Q_C, Q_B, Q_E, and Q_{SX} for a 3-D TCAD simulation of ^{16}O ions impingent outside the DT of the nominal-HBT.

As previously discussed, the heavy-ion-induced transient current and voltage at the collector terminal are responsible for the circuit-level upsets in HBT digital logic. In light of this fact, 3-D ion-strike simulations were also performed on the 3-μm internal R-HBT and the external R-HBT using the same parameters as for the nominal-HBT. $I_{C,nom}$, $I_{C,int}$, and $I_{C,ext}$ are used to denote the simulated transient current on the collector terminal of the nominal-HBT, 3-μm internal R-HBT, and external R-HBT, respectively. In a similar fashion, $Q_{C,nom}$, $Q_{C,int}$, and $Q_{C,ext}$ are used to denote the simulated collector-collected charge for the nominal-HBT, 3-μm internal R-HBT, and external R-HBT, respectively. $I_{C,nom}$, $I_{C,int}$, and $I_{C,ext}$ for an ion strike inside the DT are illustrated Figure 100(a).

The peak values of $I_{C,int}$ and $I_{C,ext}$ are actually larger than the peak value of $I_{C,nom}$. This observation can be attributed to the fact that radiation-induced substrate potential modulation turns on the parasitic BJT that is formed between the n-ring, substrate, and collector. Under steady-state bias conditions (V_{SX}=-4 V, V_{NR}=0 V or 4 V, and V_C=0 V), this parasitic BJT is in cut-off mode since both pn-junctions are reverse biased. In the

aftermath of an ion strike, the substrate potential contours along the heavy-ion track are such that the parasitic BJT is turned on, thereby enabling a direct conduction path from the n-ring to the collector. This process is responsible for the observed amplification of both $I_{C,int}$ and $I_{C,ext}$ for ^{16}O ion strikes inside the DT.

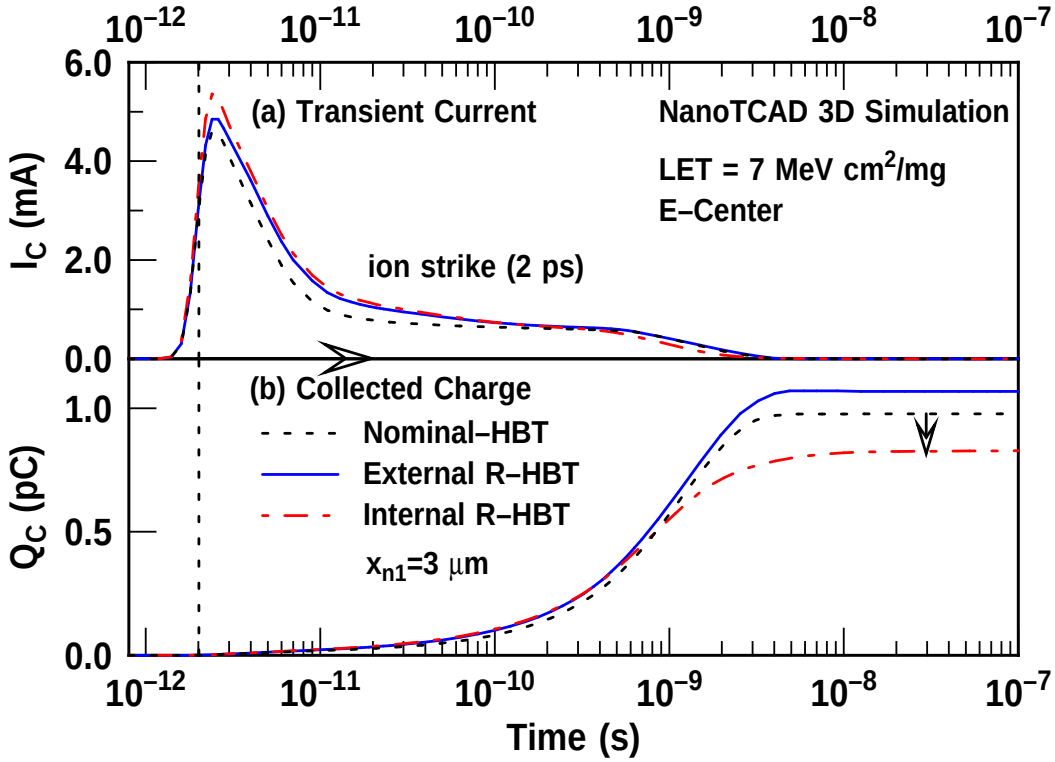

Figure 100: (a) $I_{C,nom}$, $I_{C,int}$, and $I_{C,ext}$; and (b) $Q_{C,nom}$, $Q_{C,int}$, and $Q_{C,ext}$ for a 3-D TCAD simulation of ^{16}O ions impingent inside the DT.

Moreover, the peak value of $I_{C,int}$ is greater than the peak value of $I_{C,ext}$ since there is no DT boundary located between the n-ring and sub-collector of the internal R-HBT. Approximately 9 ns after the ion strike, $I_{C,int}$ decreases faster than either $I_{C,ext}$ or $I_{C,nom}$. This reduction in $I_{C,int}$ occurs as electrons are shunted away from the sub-collector to the n-ring, which is the intended effect. For high excess carrier concentrations, parasitic-BJT amplification is so dominant that internal n-ring collection does not occur until a significant number of excess carriers have been removed. Once these carriers are removed, n-ring collection continues for several nanoseconds and is responsible for the reduction in $Q_{C,int}$ depicted in Figure 100(b). It should also be noted that $Q_{C,ext}$ is actually larger than either

$Q_{C,int}$ or $Q_{C,nom}$, which can be attributed to the fact that the presence of a DT edge in between the n-ring and sub-collector limits the ability of the n-ring to collect excess electrons for an ion strike inside the DT.

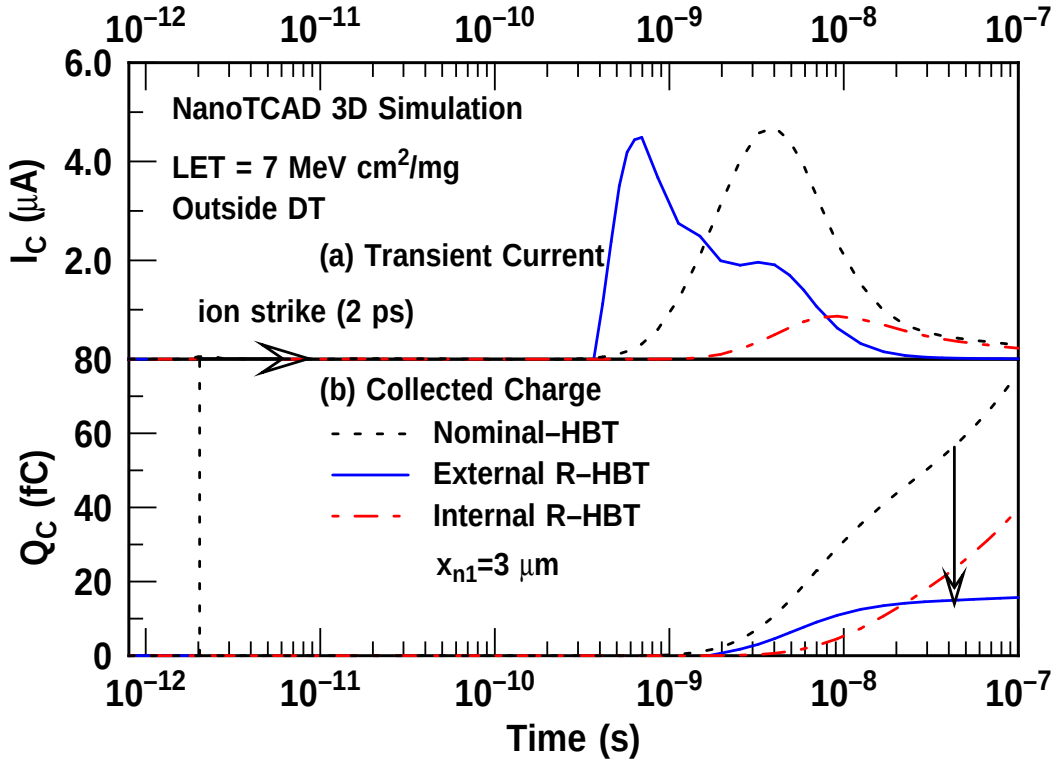

Figure 101: (a) $I_{C,nom}$, $I_{C,int}$, and $I_{C,ext}$; and (b) $Q_{C,nom}$, $Q_{C,int}$, and $Q_{C,ext}$ for a 3-D TCAD simulation of ^{16}O ions impingent outside the DT.

In Figure 101(a), $I_{C,nom}$, $I_{C,int}$, and $I_{C,ext}$ for ^{16}O ions impingent 1 μm outside the DT are illustrated. Compared to the peak $I_{C,nom}$, there is a 75% reduction in the peak value of $I_{C,int}$ in addition to a delay in the onset of $I_{C,int}$. These observations are a result of the fact that the DT edge of the 3 μm-internal R-HBT is located 5 μm away from the edge of the sub-collector. Therefore, a heavy ion impingent 1 μm outside the DT of the 3 μm-internal R-HBT is actually further away from the sub-collector than one impingent 1 μm outside the DT of the nominal-HBT or external R-HBT. Although the peak value of $I_{C,ext}$ is equal to the peak value of $I_{C,nom}$, the rate of increase of $I_{C,ext}$ is significantly faster than that of $I_{C,nom}$. More importantly, once $I_{C,ext}$ reaches its peak value the rate of decrease of $I_{C,ext}$ is also significantly faster than that of $I_{C,nom}$. Therefore, $I_{C,ext}$ vanishes several

nanoseconds before either $I_{C,int}$ or $I_{C,nom}$, which results in a $Q_{C,ext}$ that is approximately equal to $0.2 \times Q_{C,nom}$ at 100 ns after the ion strike, as shown in Figure 101(b).

A comparison of the measured (open symbols) and simulated (closed symbols) values of $Q_{C,nom}$, $Q_{C,int}$, and $Q_{C,ext}$ is shown in Figure 102. Each simulated value of Q_C is representative of the time integral of the corresponding I_C of over 14 μs. There is reasonably good agreement in the values of Q_C for ^{16}O ion strikes inside the DT, while for ion strikes outside the DT there is some deviation between the simulated and measured results.

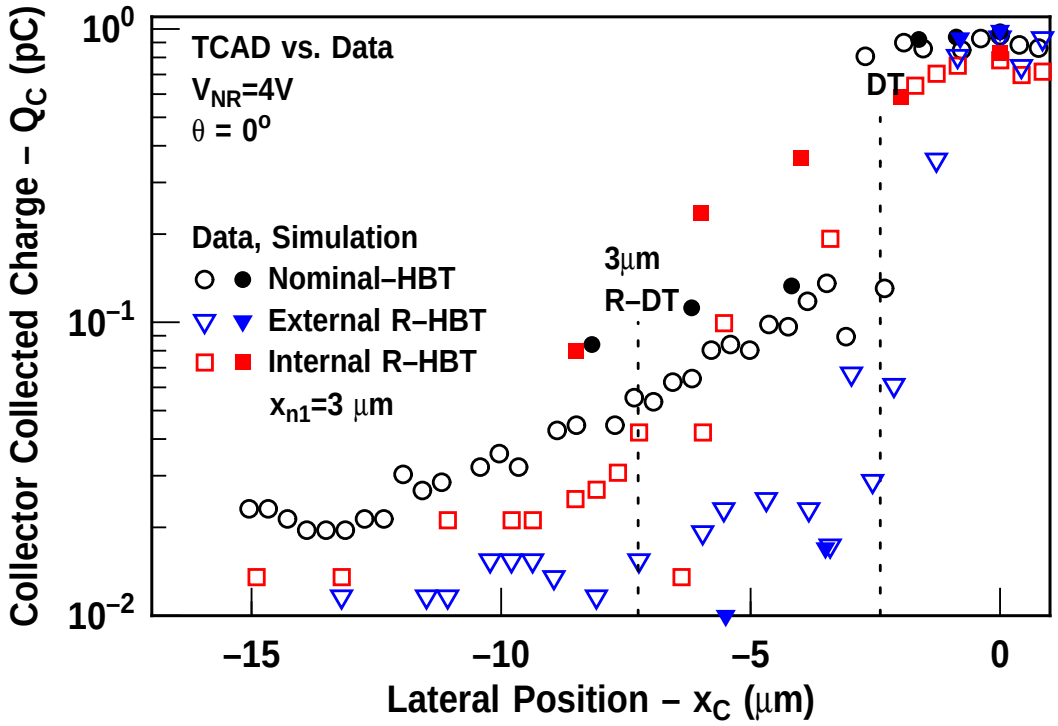

Figure 102: Comparison of the ^{16}O microbeam irradiation data and 3-D TCAD simulation of $Q_{C,nom}$, $Q_{C,int}$, and $Q_{C,ext}$.

7.5 Conclusion

An experimental evaluation of several transistor-level layout-based RHBD techniques for SEE mitigation in 3rd-generation SiGe HBTs has been presented, and the results have been verified using 3-D charge-collection simulations. In the best-case scenario, reductions of 53% and 21% have been observed for the spatially-integrated collector-collected charge and peak collector-collected charge, respectively. These results were obtained on two different

RHBD variants and compare well with the reductions achieved via employing epitaxial substrates [360], but are substantially higher than the reductions achieved by using SiGe HBTs on SOI [372].

In the case of ^{16}O ion strikes inside the DT, the collector-collected charge of all RHBD variants are still larger than the typical 100 fC circuit-level critical charge (Q_{crit}) of HBT digital logic [331]. Conversely, if the ion strikes are located outside the DT, then the collector-collected charge of the external R-HBT approaches the range of typical Q_{crit} values, which is clearly encouraging news. Assuming that carrier diffusion lengths are on the order of 100 μm or more, which extend well outside the DT, there is a considerable amount of charge that could potentially be diverted away from the substrate-to-sub-collector junction in a heavy-ion broadbeam environment.

The minimum spacing requirement of 2 μm between the n-ring and sub-collector for 3rd-generation SiGe HBTs may be overcome by reducing both the BEOL thermal cycles and the sub-collector doping, both of which are easily done in other technology platforms. Another viable approach to SEE mitigation may involve the combination of process-based and layout-based RHBD approaches. To be sure, it should be emphasized that a strictly layout-based RHBD technique has the desirable advantage of being more cost effective than these process-based approaches. Furthermore, the layout-based approaches do not incur the increases in circuit area and power consumption that are common to many circuit-based approaches and have been successful in SEU mitigation for CMOS technology platforms [373]. Ultimately, the success of any SEE mitigation technique will be determined by the cross section vs. LET response obtained via the heavy-ion broadbeam analysis of HBT digital logic.

CHAPTER 8

LASER-INDUCED HBT CURRENT TRANSIENTS

8.1 Introduction

In Chapter 5, the results of single-photon pulsed laser irradiation were used to quantify the SEU response of several circuit-based RHBD techniques to HBT digital logic. Although single-photon pulsed laser irradiation is less destructive and less expensive than heavy-ion microbeam irradiation, there are several situations in which the physical limitations of single-photon absorption (SPA) limit its use in SEE analysis. One of the major limitations of SPA is the fact that the intensity of the laser beam exponentially decreases as a function of depth into the target material, which also translates into an exponential decrease in the laser-generated excess carrier concentration as a function of depth. Furthermore, if the laser is focused on the topside of the die, then the metal and dielectric layers located over the circuit cause additional non-uniform beam attenuation. These factors introduce uncertainties in the determination of the excess carrier concentration as a function of depth, thereby hampering the investigation of depth-dependent SEE phenomena at the transistor level.

In this chapter, an investigation of charge-collection phenomena using a two-photon absorption (TPA) technique is presented. Using two-photon pulsed laser irradiation, it is possible to generate Gaussian-distributed excess carrier concentrations with excellent 3-D resolution. This capability is leveraged to analyze the depth dependence of the transistor-level layout-based RHBD techniques that were introduced in the previous chapter. In the first section, basic TPA theory is introduced, and the experimental details are presented next, with a focus on the custom-made broadband packaging solution and the parameters of the two-photon pulsed laser system. In the third section, the transient current waveforms of the nominal-HBT are presented with an emphasis on the impact of the lateral and vertical position of the laser focal spot on the waveforms. In the fourth section, this analysis is

repeated for the external R-HBT, with the additional considerations of the impact of the n-ring voltage and laser pulse energy. The chapter is then concluded with a discussion of the implications for SEE mitigation in bulk SiGe HBTs.

8.2 Two-Photon Absorption

In single-photon pulsed laser irradiation, photons with an energy greater than the bandgap ($E_{ph} \ggg E_g$) are directed onto the topside of the die. This orientation results in a laser-generated excess carrier concentration that exponentially decreases as a function of the distance from the die surface. This relationship results from the exponential decrease in the laser intensity as a function of depth into the material according to Beer's Law, which can be written as [374]

$$A_\lambda = -\log\left(\frac{I}{I_0}\right) = \epsilon_\lambda bc, \tag{102}$$

where A_λ is the optical absorbance, I_0 is the light intensity at the surface, I is the light intensity in the material, ϵ_λ is the molar absorptivity, b is the path length, and c is the concentration of the target material.

Single-photon pulsed laser irradiation is typically performed in a manner that reduces higher-order effects [221][375]. Since the absorption coefficient in Si is several orders of magnitude lower at infrared than at visible wavelengths, there is no e-h pair creation for sub-bandgap photons ($E_{ph} \lll 1.12$ eV) at low light intensity [376]. As the light intensity is increased, two sub-bandgap photons can be simultaneously absorbed to generate a single e-h pair [225]. In this regime, the concentration of laser-generated excess carriers is proportional to I^2, which means that excess carriers are generated where the beam intensity is high, and the attenuation associated with Beer's law can be neglected [377]-[379]. This localized confinement translates into a precise and deterministic mapping of laser-generated excess carriers in the 3-D volume containing the transistor.

TPA theory is now explained following the discussion in [225]. The 3-D laser-induced excess carrier concentration ($N(r,z)$), generated via either SPA or TPA, can be described as [377]

$$\frac{dN\left(r,z\right)}{dt} = \frac{\alpha I\left(r,z\right)}{E_{ph}} + \frac{\beta_2 I^2\left(r,z\right)}{2E_{ph}}, \tag{103}$$

where α is the linear absorption coefficient and β_2 is the TPA coefficient. I can be written as

$$I(r,z) = \frac{2P}{\pi\omega^2}\exp\left(\frac{-2r^2}{\omega^2}\right), \tag{104}$$

where P is the laser pulse power, ω is the beam radius, and r and z are polar coordinates. P is obtained by dividing the laser pulse energy by the pulse width, and ω can be written as

$$\omega(z) = \omega_0\left[1+\left(\frac{\lambda z}{\pi\omega_0^2 n}\right)^2\right]^{1/2}, \tag{105}$$

where λ is the photon wavelength, z is the depth into the target material, n is the refractive index, and ω_o is the radius of the laser focal spot.

In SPA, I is so small that the second term in (103) can be neglected, and the SPA-induced excess carrier concentration (N_{1P}) can be written as

$$N_{1P}(z) = \frac{\alpha}{E_{ph}}\exp\left(-\alpha z\right)\int_{-\infty}^{\infty} I_0(z,t)dt. \tag{106}$$

Nevertheless, the TPA-induced excess carrier generation is affected by non-exponential attenuation and non-linear refraction, both of which perturb beam propagation into the substrate. If non-linear absorption dominates the energy loss mechanisms, then the TPA-induced excess carrier concentration (N_{2P}) can be expressed as

$$N_{2P}(z) = \frac{\beta_2}{2E_{ph}}\int_{-\infty}^{\infty} I^2\left(z,t\right)dt, \tag{107}$$

where I is now given as

$$I(z) = \frac{I_0}{1+\beta_2 I_0 z}. \tag{108}$$

8.3 Experiment Details

8.3.1 Backside TPA Packaging

Two-photon pulsed laser irradiation was performed on the nominal-HBT and the external R-HBT, both of which were introduced in Chapter 7. The transistors were mounted into a custom-made package, which was designed to accommodate both topside and backside laser irradiation. The packaging solution and experimental setup for backside pulsed laser irradiation are illustrated in Figure 103.

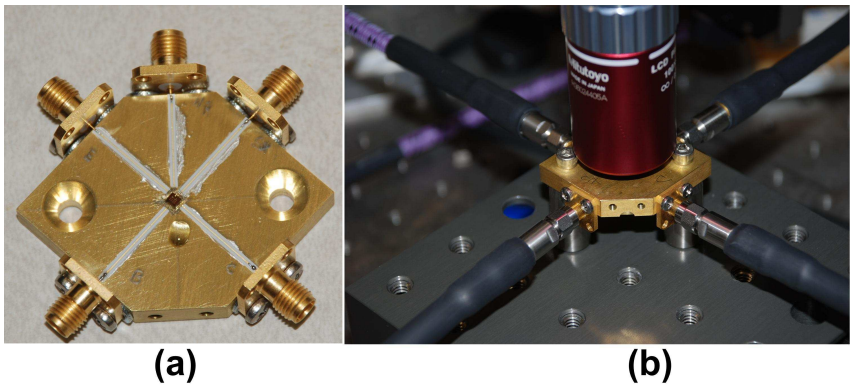

Figure 103: (a) Brass block for backside two-photon pulsed laser irradiation and (b) pulsed laser irradiation setup.

The broadband package was fabricated out of an alloy-360 brass rod that was machined into a six-terminal hexagonal brass block, forming the ground plane. To enable backside irradiation, a 1-mm diameter hole, positioned at the center of a 10-mm countersink, was drilled through the block. Custom-designed *dc*-macros were diced out of a 5×5 mm^2 die into a 2×2 mm^2 block and secured to the brass block using non-conductive epoxy, which is required for the isolation of the Si substrate from the brass material. Using a 1-mil gold wire that is less than 1 mm in length, each transistor terminal was wire bonded to a polished alumina transmission line measuring 10×50×800 mil^2. The transmission lines were coated on the top with 9.57-mil wide gold strips and on the bottom with 50-mil wide gold strips. These components result in a .25 dB loss and a characteristic impedance of 49.65 Ω at 15 GHz. The transmission lines were attached to the brass block with conductive silver epoxy and soldered to 18 GHz stainless-steel SMA connectors. 2.9 mm coaxial cables, with a bandwidth of 40 GHz, were used to connect these SMA launchers to a Tektronix 12 GHz TDS6124C real-time digital storage oscilloscope, and 40 GHz bias tees were used to apply the appropriate voltage to the transistor terminals.

8.3.2 Two-Photon Pulsed Laser Irradiation

The laser pulse energy was controlled using a variable optical attenuator without neutral density filters (OD-0) and was monitored using a large-area InGaAs photo diode. At 0D-0, the conversion factor between the photo-diode response and pulse energy is 845.6 pJ/mV.

The refractive losses (I_r/I_0) at the Si surface can be written as

$$\frac{I_r}{I_0} = \frac{(n_2 - n_1)^2}{(n_2 + n_1)^2}, \tag{109}$$

where n_1=1 is the refractive index of air and n_2=3.5 is the refractive index of Si, which together yield a refractive loss of 31% if free-carrier absorption and beam phase effects are neglected. The two-photon pulsed laser parameters are given in Table 9.

Table 9: Two-photon pulsed laser system parameters.

Pulse Width	120 fs
Wavelength	1260 nm (0.98 eV)
Laser Repetition Rate	1 kHz
Focal Spot Size ($2\omega_0$)	1.6 μm
Laser Pulse Energy (PE)	11.9, 16.6, 26.1, 32.1 nJ

The laser-induced excess carrier concentration is a function of the pulse energy, pulse width, ω_0, and β_2 [225]. These excess carriers are concentrated in the region where the beam intensity is highest, thereby forming a cigar-shaped charge cloud that is centered at the focal point of the beam, as shown in Figure 104.

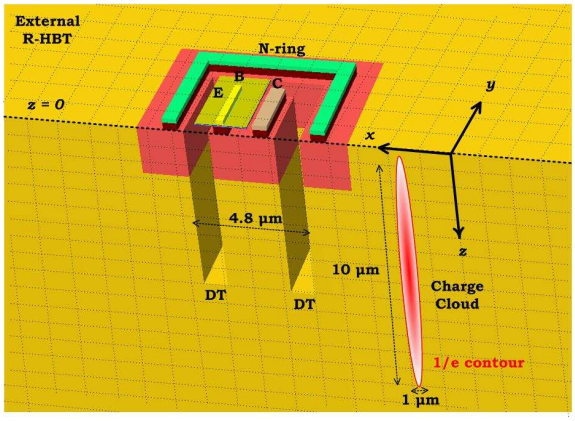

Figure 104: Schematic of the 1/e contour of TPA-induced charge deposition around the external R-HBT.

Using a β_2 value of 0.1 cm, which is justified by the results in [225], the $1/e$ elliptical contour that bounds the excess carrier concentration measures approximately 1×10 μm^2 in Si for the laser parameters in Table 9. If beam depletion and higher-order non-linear optical effects are neglected, then the $1/e$ contour depends only on ω_0 and n.

Transistors were irradiated with the n-ring, collector, base, and emitter terminals grounded and with -4 V applied to the substrate. Transient waveforms were collected on the n-ring, collector, and substrate and were manually saved to the hard drive of the Tektronix scope. Stage control in the x-y plane was provided via a custom-built LabVIEW program, and focal positioning the in the z-direction was achieved by manually tuning the objective lens, locking in that position as '0,' and using a separate precision controller to increment the focal point with sub-micron resolution.

8.4 Laser-Induced Current Transients in the Nominal-HBT

8.4.1 Lateral Position Dependence of the Laser Focal Spot

Two-photon pulsed laser irradiation at the topside Si surface was performed by first manually focusing the laser focal spot to the backside Si surface and then moving the focal point through the substrate until the transistor is brought into focus on the CCD imaging system. Once the transistor is in focus, the position of the focal spot is fine tuned by making small adjustments until the largest current transients are observed on the collector and substrate terminals. At this position, hereafter denoted as z=0 μm, the impact of the lateral position of the focal spot on terminal-collected charge can be investigated by simply moving the focal spot in the x-y plane and collecting current transients both inside and outside the DT.

The transient current waveforms on the collector (I_C) and substrate (I_{SX}) during two-photon pulsed laser irradiation of the nominal-HBT at a laser pulse energy of 16.6 nJ are illustrated in Figure 105. At these conditions, neither the base nor emitter terminal generated any current transient waveforms. Inside the DT, I_C and I_{SX} exhibit a classical "double-exponential" shape, which is characterized by a prompt initial response with a fast rise time (τ_r <0.1 ns) and a sharp peak, followed by a delayed response with a large fall time (τ_f >2 ns). Outside the DT, I_C and I_{SX} exhibit the same functional form as was observed inside the DT, with the exception that the rise time on the leading exponential is longer, and there is a 67% reduction in the peak current transient on the collector ($I_{C,Peak}$) and substrate ($I_{SX,Peak}$) terminals.

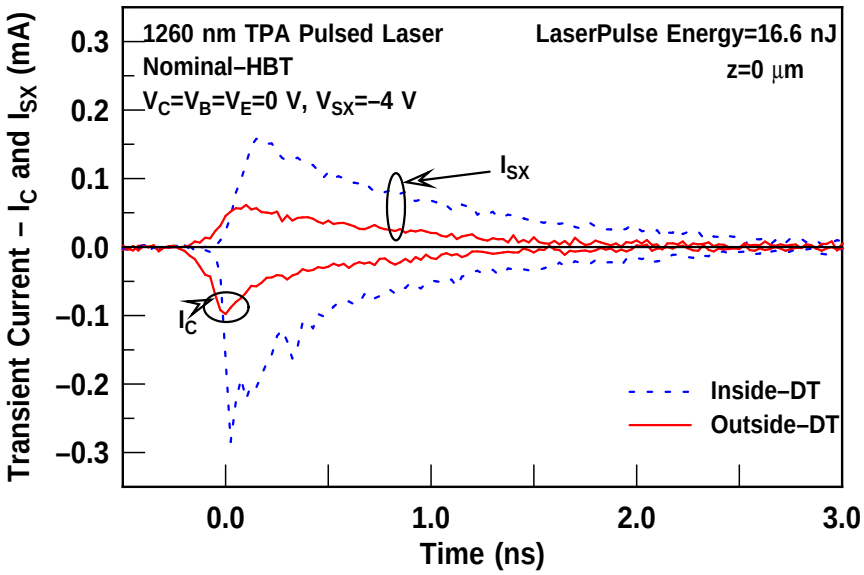

Figure 105: I_C and I_{SX} inside and outside the DT of the nominal-HBT at z=0 μm.

As the laser focal spot was stepped along the y-coordinate of Figure 104, I_C and I_{SX} were collected across the length of the transistor. The time integral of I_C and I_{SX} was used to determine the laser-induced collector- and substrate-collected charge, Q_C and Q_{SX}, respectively. In Figure 106, Q_C, Q_{SX}, $I_{C,peak}$, and $I_{SX,peak}$ are plotted as a function of the lateral position across the transistor (y). The y-coordinate here is equivalent to the x_C-coordinate that was used to analyze the heavy-ion microbeam data in Chapter 7. In this chapter, the absolute values of Q_C and $I_{C,Peak}$, which are both negative, are plotted for convenience.

Q_C is approximately equal to Q_{SX} for irradiation both inside and outside the DT, which suggests that the collector and substrate terminals dominate the collection of electrons and holes, respectively. These results are consistent with the results from heavy-ion microbeam irradiation, which are shown in Figure 89, and 3-D charge collection-simulation results, which are shown in Figure 98. $I_{C,Peak}$ is 85% larger than $I_{SX,Peak}$ inside the DT and 57% larger than $I_{SX,Peak}$ outside the DT. This result suggests that the collection of electrons by the collector is faster than the collection of holes by the substrate. The duration of the current transients is characterized by measuring the full-width at half-maximum (FWHM) and full-width at tenth-maximum (FWTM).

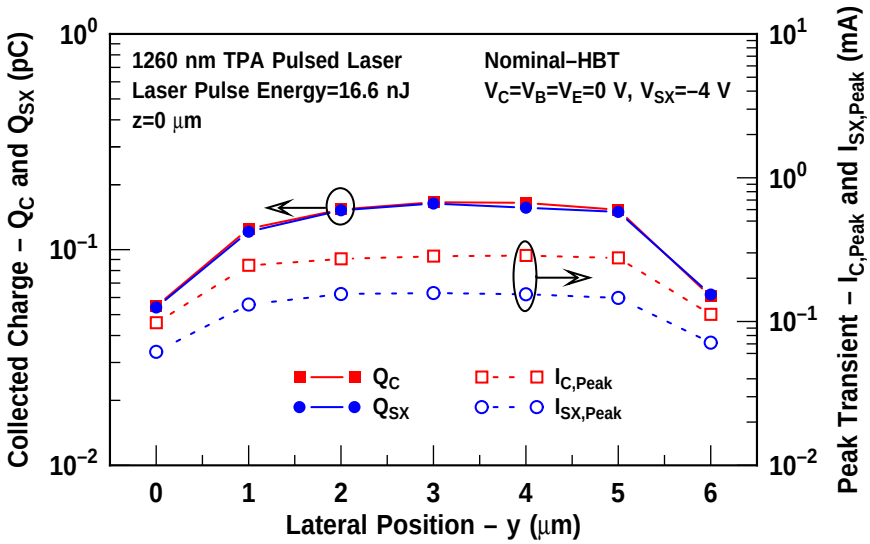

Figure 106: Q_C, Q_{SX}, $I_{C,peak}$, and $I_{SX,peak}$ vs. y for the nominal-HBT at z=0 μm.

In Figure 107, the FWHM and FWTM of the collector and substrate terminals of the nominal-HBT are plotted as a function of y. The FWTM of I_{SX} is 150% larger than the FWTM of I_C, and the FWHM of I_{SX} is 250% larger than the FWHM of I_C.

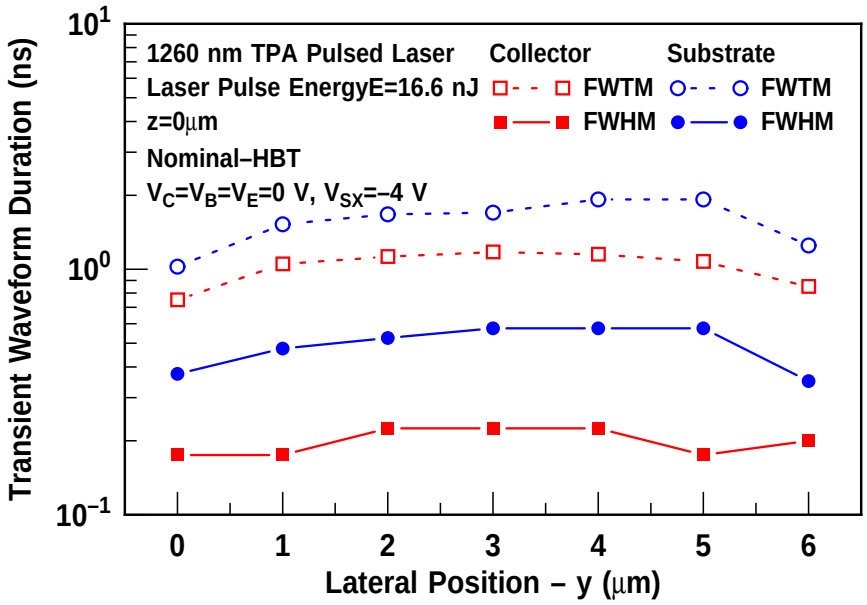

Figure 107: FWHM and FWTM of I_C and I_{SX} for the nominal-HBT at z=0 μm.

The longer time needed for the collection of holes by the substrate can be attributed to the fact that the mobility of holes in Si is less than that of electrons coupled with the fact

that the substrate contacts are located least 10 μm away from the transistor.

8.4.2 Vertical Position Dependence of the Laser Focal Spot

In this section, the impact of the vertical position of the laser focal spot on I_C and I_{SX} is investigated. First, the focal spot was positioned near the surface of the active area, then z was set to 0 μm, and the laser focal spot was moved vertically through the substrate. Positive values of z denote a focal spot located below the topside Si surface, and larger values of z denote a focal spot that is closer to the backside Si surface.

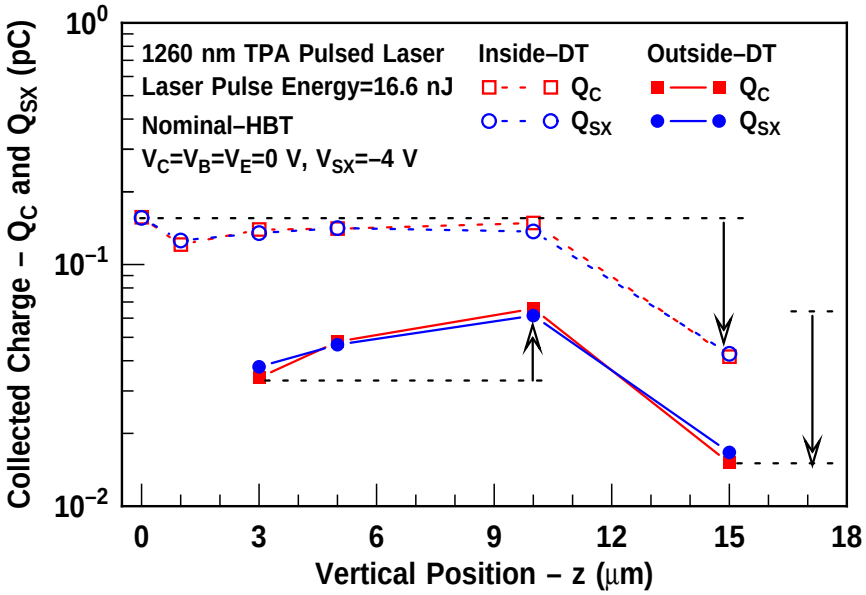

Figure 108: Q_C and Q_{SX} vs. z inside and outside the DT of the nominal-HBT.

As was observed at the surface, Q_C is approximately equal to Q_{SX} up to a depth of z=15 μm. Inside the DT, Q_C and Q_{SX} both decrease by between 5% to 23% as the laser focal spot is moved from the surface to z=10 μm. At a depth of z=15 μm, Q_C and Q_{SX} both decrease by over 70%, compared to the correpsonding values at z=10 μm. Conversely, if the focal spot is positioned outside the DT, then as the focal spot is moved from z=3 μm to z=10 μm, Q_C and Q_{SX} increase by 41% and 77%, respectively. As the focal spot is moved further down, to a depth of z=15 μm, Q_C and Q_{SX} both decrease by over 55%. There were no current transients observed at a depth of z=20 μm. When the laser focal spot is positioned outside the DT, the increases in Q_C and Q_{SX} as a function of z are

driven by increases in both the peak magnitude and duration of the corresponding current transients.

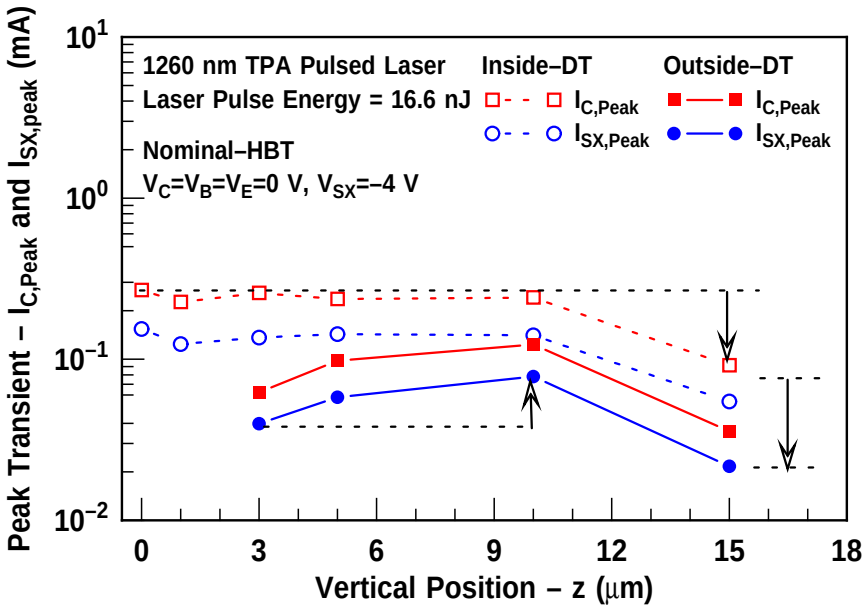

Figure 109: $I_{C,Peak}$ and $I_{SX,Peak}$ vs. z inside and outside the DT of the nominal-HBT.

In Figure 109, $I_{C,Peak}$ and $I_{SX,Peak}$ are plotted as a function of z for pulsed laser irradiation both inside and outside the DT. Outside the DT, $I_{C,Peak}$ first increases by 98% as the focal spot is moved from a depth of z=3 μm to z=10 μm and then subsequently decreases by over 71%, as the focal spot is moved further down to z=15 μm. The corresponding variations in $I_{SX,Peak}$ are a 95% increase and a 72% decrease, respectively. Conversely, inside the DT, $I_{C,Peak}$ first decreases by 15% as the focal spot is moved from a depth of z=0 μm to z=10 μm and then subsequently decreases by up to 62%, as the focal spot is moved to z=15 μm. $I_{SX,Peak}$ displays a similar behavior.

As was observed for $I_{C,Peak}$ and $I_{SX,Peak}$, the FWTM of I_C and I_{SX} has a similar functional dependence on z, as depicted in Figure 110. Outside the DT, the FWTM of I_C increases by 80% as the laser focal spot is moved from a depth of z=3 μm to z=10 μm and then subsequently decreases by 60%, as the focal spot is moved further down to z=15 μm. In a similar fashion, the FWTM of I_{SX} increases by 22% as the focal spot is moved from a depth of z=3 μm to z=10 μm and then subsequently decreases by 73%, as the focal spot is moved further down to z=15 μm. Conversely, inside the DT, the FWTM of I_C decreases by

14% as the focal spot is moved from the surface to a depth of z=10 μm and then decreases by 51%, as the focal spot is moved further down to z=15 μm. The corresponding decreases for the FWTM of I_{SX} are 13% and 34%, respectively.

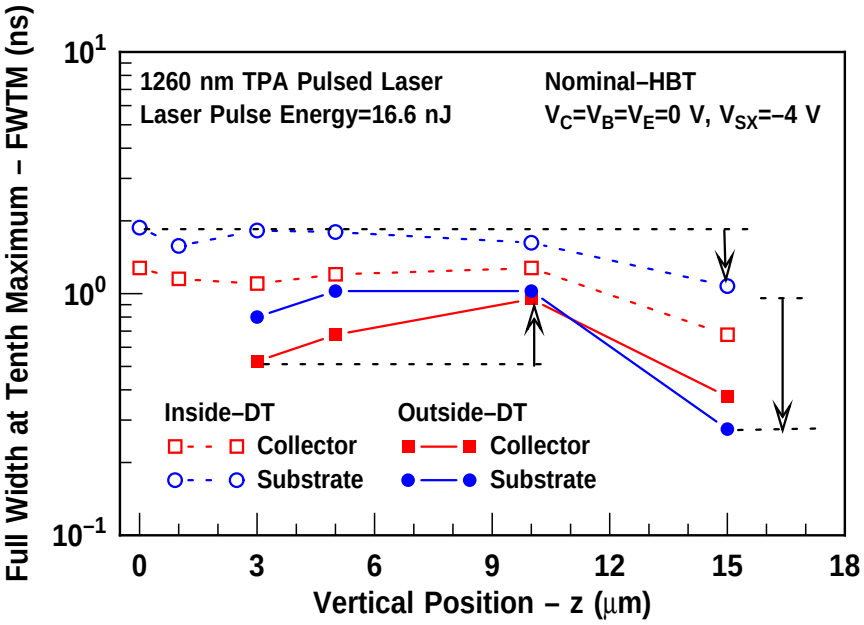

Figure 110: FWTM of I_C and I_{SX} vs. z inside and outside the DT of the nominal-HBT.

8.5 Laser-Induced Current Transients in the External R-HBT

8.5.1 Lateral Position Dependence of the Laser Focal Spot

Two-photon pulsed laser irradiation was performed on the external R-HBT to investigate the degree of SEE mitigation offered by the external n-ring as a function of the vertical and lateral position of the laser focal spot, n-ring voltage, and laser pulse energy. In this section, measurements of the laser-induced n-ring current transient (I_{NR}) are presented in addition to I_C and I_{SX}.

In Figure 111, I_C, I_{NR}, and I_{SX}, are plotted for pulsed laser irradiation inside the DT of the external R-HBT at a depth of z=1 μm and z=5 μm. As was observed for the nominal-HBT in Figure 105, $I_{C,Peak}$ is again significantly larger than $I_{SX,Peak}$, and the fall time of I_C is shorter than the fall time of I_{SX}. Interestingly, at z=1 μm, I_{NR} exhibits a positive prompt component within 1 ns that subsequently decays and gives way to a

negative component, which lasts up to 3 ns after the onset of I_{NR}.

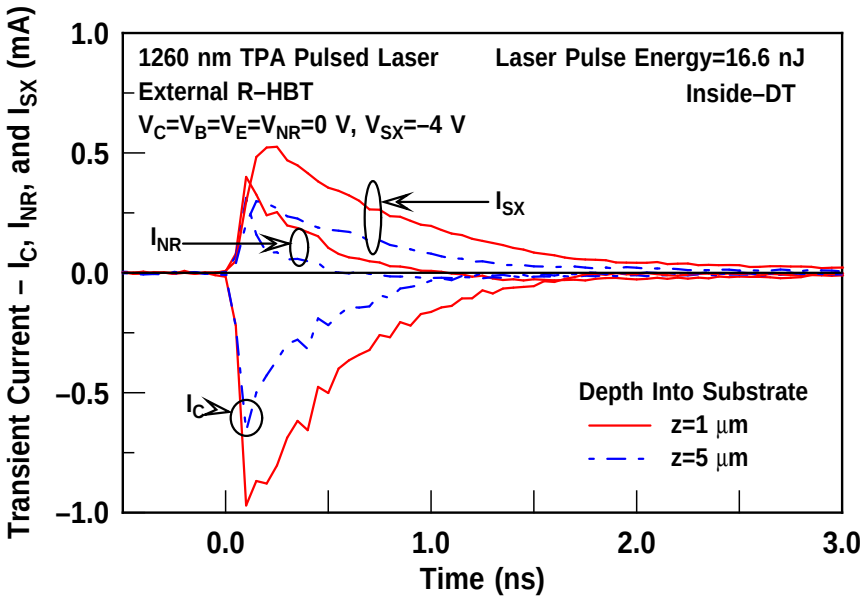

Figure 111: I_C, I_{NR}, and I_{SX} inside the DT of the external R-HBT at z=1 and 5 μm.

The "negative charge" collected by the n-ring (Q_{NR}) is calculated by taking the time integral of the negative component of I_{NR}. As was demonstrated by the 3-D TCAD charge-collection simulations in Chapter 7, this phenomenon in I_{NR} is a result of the parasitic BJT, which is formed between the n-ring (n), substrate (p), and sub-collector(n), being turned on as a result of laser-induced substrate potential modulation. In contrast to the nominal-HBT, when the laser focal spot is positioned at a depth of z=5 μm, the magnitude and duration of I_C and I_{SX} both decrease, and I_{NR} goes negative much earlier than when the focal spot is positioned at a depth of z=1 μm. In Figure 112, I_C, I_{NR}, and I_{SX} are illustrated for pulsed laser irradiation outside the DT at a depth of z=1 μm and z=5 μm.

When the laser focal spot is positioned outside the DT, at a depth of z=1 μm, I_{NR} and I_{SX} are the dominant current transients. This result is in contrast to the observations that were made when the focal spot was positioned inside the DT, in which case I_C and I_{SX} dominated the response. Outside the DT, I_{NR} and I_{SX} both have a much longer rise time, a broad peak, and a large fall time, which collectively cause the transient currents to last much longer than 3 ns. Conversely, I_C still has a small rise time, a sharp peak, and a rapidly decaying tail of the same form as observed for pulsed laser irradiation inside the

DT.

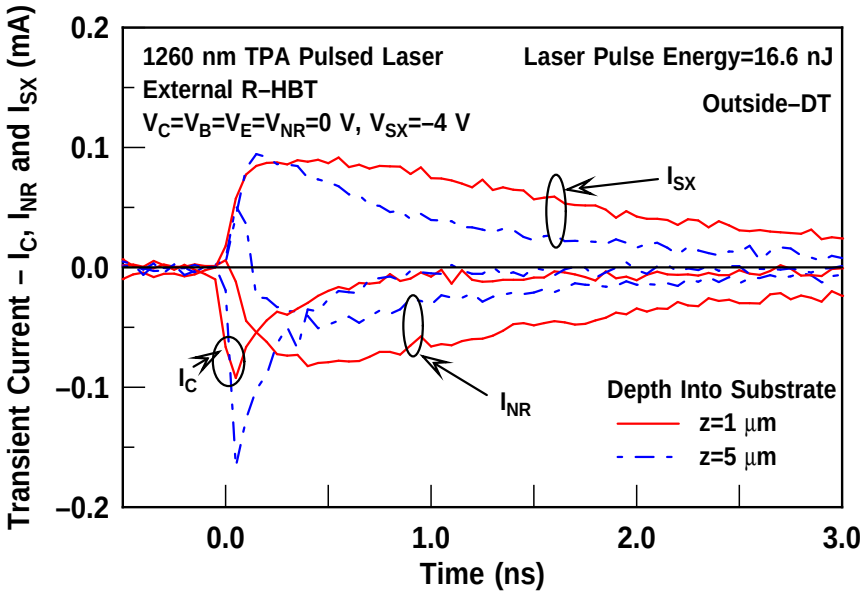

Figure 112: I_C, I_{NR}, and I_{SX} outside the DT of the external R-HBT at z=1 and 5 μm.

8.5.2 Vertical Position Dependence of the Laser Focal Spot

In Figure 113, I_{NR} is illustrated for the laser focal spot positioned inside the DT of the external R-HBT at depths ranging from z=1 μm to 15 μm.

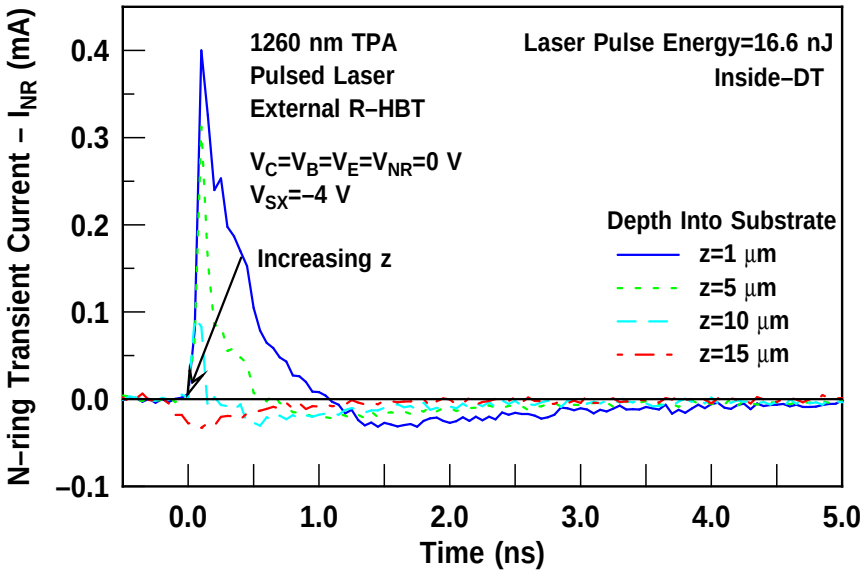

Figure 113: z dependence of I_{NR} inside the DT of the external R-HBT.

As the focal spot is moved deeper into the substrate, the potential modulation that turns on the parasitic BJT is less severe, and the positive component of I_{NR} decreases as z is increased. When the focal spot is at a depth of z=15 μm, the positive component of I_{NR} is completely eliminated, and Q_{NR} is entirely negative, which is the intended effect of the external n-ring.

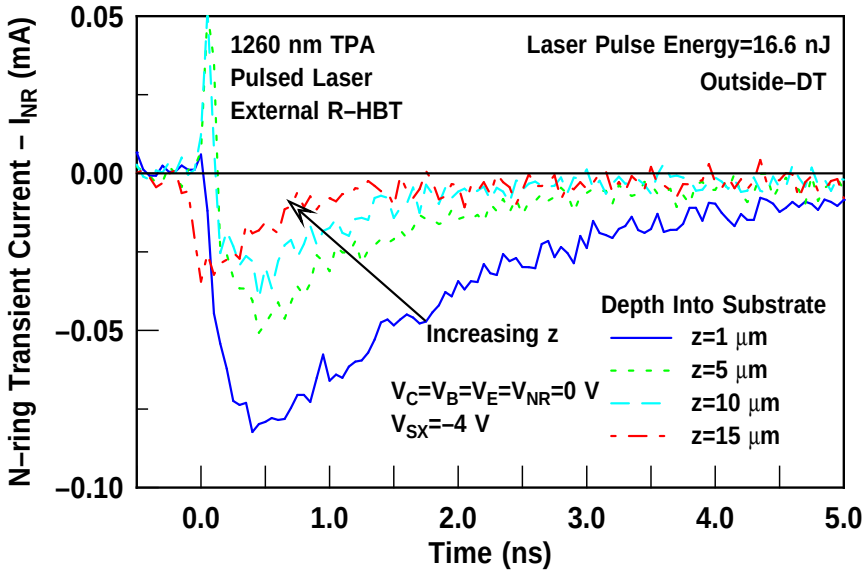

Figure 114: z dependence of I_{NR} outside the DT of the external R-HBT.

In Figure 114, I_{NR} is illustrated for the laser focal spot positioned outside the DT of the external R-HBT at depths ranging from z=1 μm to 15 μm. When the focal spot is positioned outside the DT and near the surface, at z=1 μm, the cigar-shaped charge cloud is in the $n+$ region of the external n-ring and parasitic-BJT effects are negligible. As the focal spot is moved below the substrate-to-n-ring junction, which occurs for depths ranging from z=5 μm to 15 μm, a sharp positive component of I_{NR} is established prior to the slower negative component, which is quite similar to the shape of I_{NR} observed for pulsed laser irradiation inside the DT. It should be noted, however, that the observed I_{NR} for pulsed laser irradiation outside the DT is dominated by the negative component, in contrast what was observed for irradiation inside the DT.

In Figure 115, Q_C, Q_{NR}, and Q_{SX} are plotted as a function of z for pulsed laser irradiation both inside and outside the DT of the external R-HBT. If the focal spot is

positioned inside the DT and near the surface, defined as $z \leqslant 5$ μm, then the collection of electrons is dominated by the collector, as evidenced by the fact that Q_C is approximately equal to Q_{SX}. This result is similar to what is observed for the nominal-HBT, as was shown in Figure 108. When the focal spot is positioned in this region, the external n-ring collects only 24% of the charge collected on either the collector or substrate. Conversely, when the focal spot is positioned outside the DT and near the surface, electrons are primarily collected by the external n-ring and substrate terminals, as evidenced by the fact that Q_{NR}, instead of Q_C, is now approximately equal to Q_{SX}. As illustrated in Figure 112, the final value of Q_{NR} is dominated by the long tail at the end of the current transient, which lasts up to 3 ns after the peak. When the focal spot is positioned in this region, the value of Q_C is only 30% that of Q_{NR} or Q_{SX}, which is obviously good news.

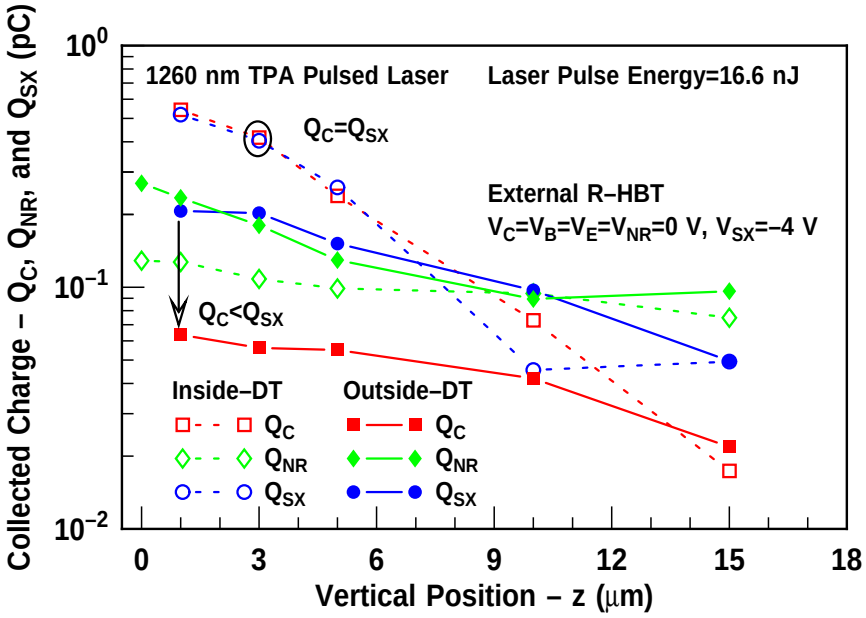

Figure 115: Q_C, Q_{SX}, and Q_{NR} vs. z inside and outside the DT of external R-HBT.

8.5.3 Impact of the N-ring Voltage

In Figures 116 and 117, I_C, I_{NR}, and I_{SX} are illustrated for pulsed laser irradiation with the focal spot positioned at a depth of z=5 μm and at V_{NR}=0 V and 4 V, both inside and outside the DT, respectively. The results for pulsed laser irradiation inside the DT are presented first. As V_{NR} is increased from 0 V to 4 V, the magnitude of the positive

component of I_{NR} is reduced, and I_{NR} goes negative for a longer period of time. Moreover, at V_{NR}=4 V, there is a corresponding reduction in the peak magnitude and duration of both I_C and I_{SX}. These results suggest that for the same amount of laser-induced substrate potential modulation, if V_{NR} is increased, then there is a reduction in the severity of the parasitic-BJT effect, and fewer electrons flow from the external n-ring to the collector. Since the parasitic-BJT effect is a strong function of the vertical position of the laser focal spot, as was illustrated in Figure 113, the degree to which V_{NR} influences this behavior is amplified when the focal spot is located closer to the surface. When the focal spot is in this position, increasing V_{NR} from 0 V to 4 V results in reductions of 44% and 37% in Q_C and Q_{SX}, respectively.

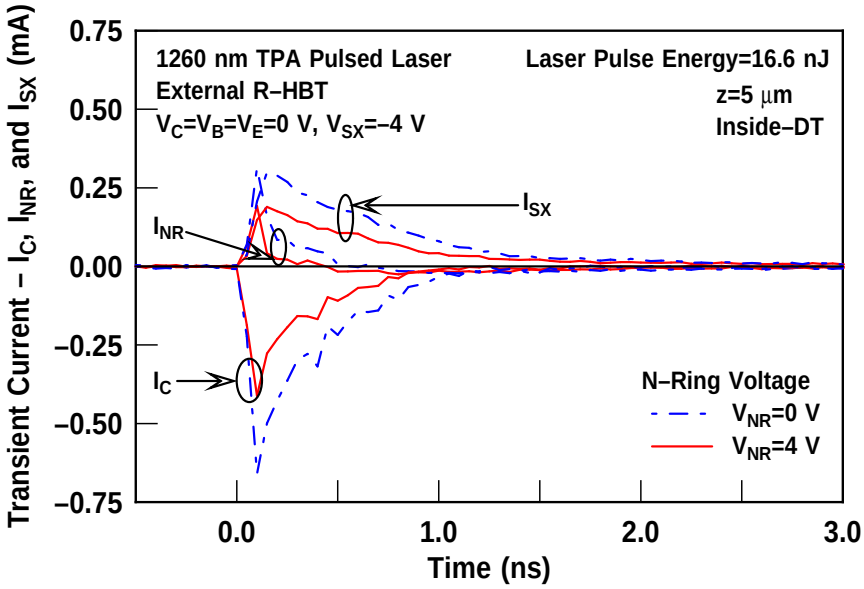

Figure 116: V_{NR} dependence of I_C, I_{NR}, and I_{SX} inside the DT of the external R-HBT.

In Figure 117, I_C, I_{NR}, and I_{SX} are illustrated for pulsed laser irradiation with the laser focal spot positioned outside the DT at a depth of z=5 μm and with V_{NR}=0 and 4 V. In this case, increasing V_{NR} does very little to mitigate either the peak magnitude or duration of both I_C and I_{SX}, and the reductions in Q_C and Q_{SX} are 12.4% and 5.8%, respectively. Moreover, increasing V_{NR} does not impact the parasitic-BJT when the focal spot is positioned outside the DT at a depth of z=5 μm, which is contrary to what is observed when the focal spot is positioned inside the DT.

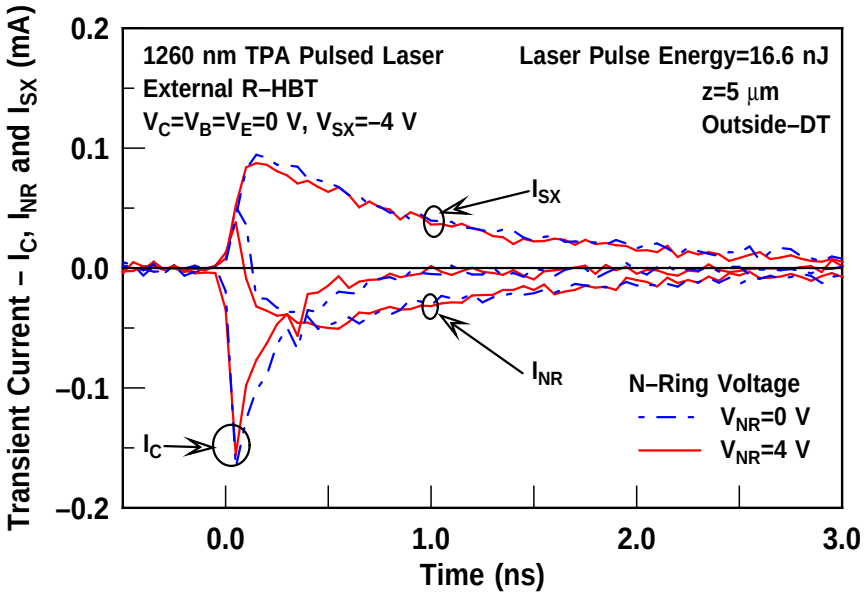

Figure 117: V_{NR} dependence of I_C, I_{NR}, and I_{SX} outside the DT of the external R-HBT.

8.5.4 Impact of the Laser Pulse Energy

In Figure 118, I_C, I_{NR}, and I_{SX} are illustrated for pulsed laser irradiation with the laser focal spot positioned inside the DT at a depth of z=5 μm and at pulse energies of 16.6 nJ and 32.0 nJ.

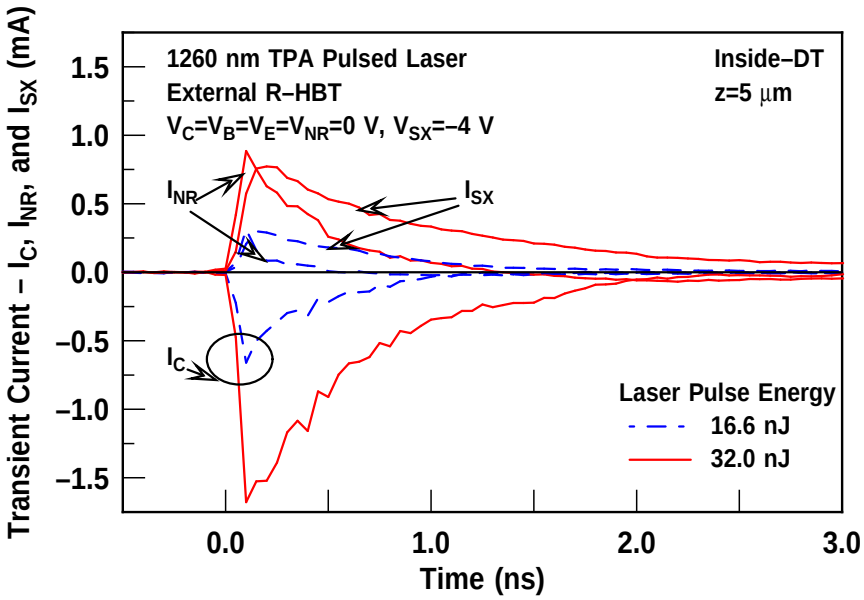

Figure 118: I_C, I_{NR}, and I_{SX} inside the DT of the external R-HBT at 16.6 and 32.0 nJ.

As the laser pulse energy is doubled from 16.6 nJ to 32.0 nJ, N_{2P} increases, which results in a dramatic enhancement in both the peak magnitude and duration of I_C and I_{SX}. In Figure 119, the dependence of I_{NR} on pulse energy is illustrated. At higher pulse energies, the parasitic BJT effect is significantly enhanced, as evidenced by the fact that the positive component of I_{NR} has a peak magnitude exceeding that of I_{SX}.

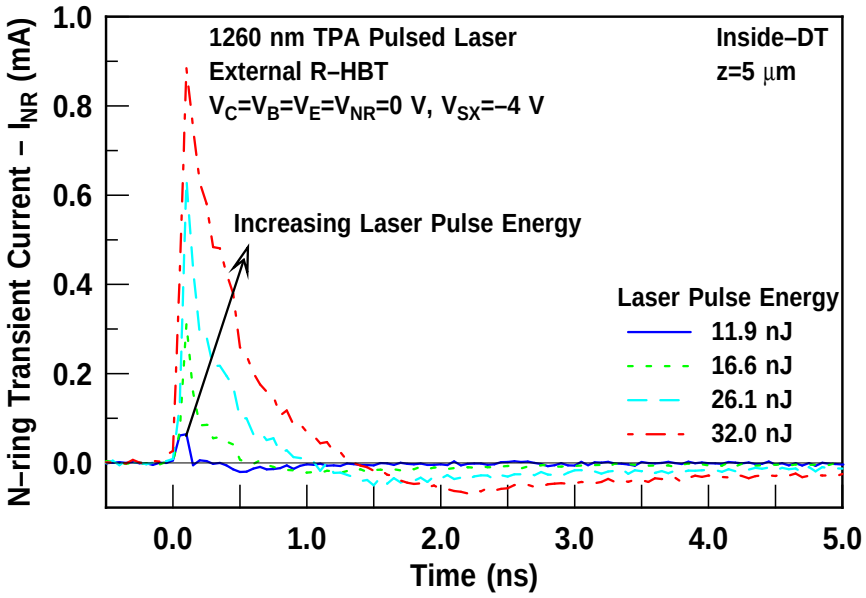

Figure 119: Pulse-energy dependence of I_{NR} inside the DT of the external R-HBT.

In Figure 120, I_C, I_{NR}, and I_{SX} are illustrated for pulsed laser irradiation outside the DT with the laser focal spot positioned at z=5 μm and at laser pulse energies of 16.6 nJ and 32.0 nJ. An increase in the laser-generated excess charge outside the DT yields even more dramatic increases in both the peak magnitude and duration of I_C and I_{SX}. At laser pulse energies of 11.8 nJ and 16.6 nJ, parasitic BJT action outside the DT is negligible, however, as the laser pulse energy is increased to 32.0 nJ, a sharp positive component of I_{NR} is observed, as shown in Figure 121. With the focal spot positioned outside the DT at a pulse energy of 32.0 nJ, the magnitude of this positive component of I_{NR} is roughly half the magnitude of the positive component of I_{NR} when the focal spot is positioned inside the DT. Furthermore, when the focal spot is positioned outside the DT, the negative component of I_{NR} has a much larger magnitude and duration than when the focal spot is positioned inside the DT.

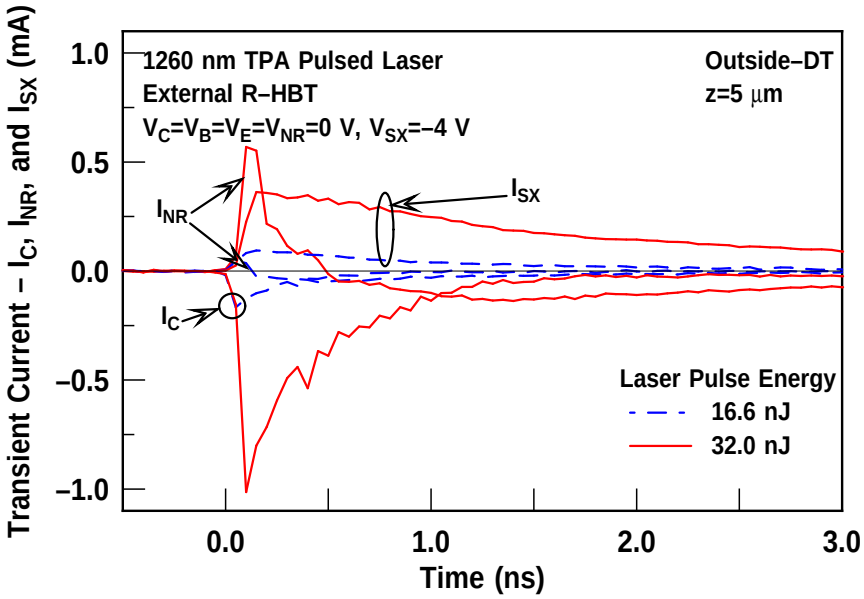

Figure 120: I_C, I_{NR}, and I_{SX} outside the DT of the external R-HBT at 16.6 and 32.0 nJ.

Moreover, it should be emphasized that the magnitude of the negative component of I_{NR} exceeds the magnitude of I_C approximately 1 ns after collection begins and remains that way for up to 5 ns, as shown in Figure 120.

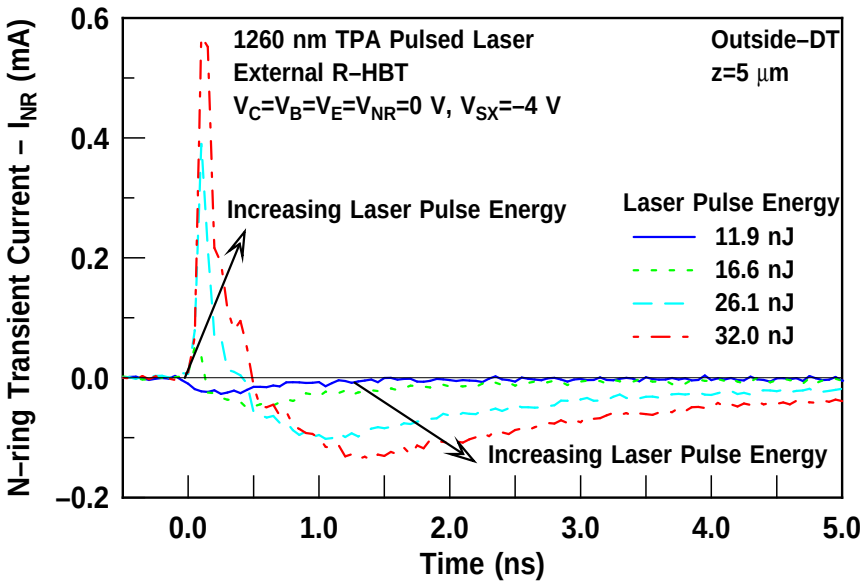

Figure 121: Pulse-energy dependence of I_{NR} outside the DT of the external R-HBT.

In Figure 122, Q_C, Q_{NR}, and Q_{SX} are plotted as a function of laser pulse energy

for irradiation both inside and outside the DT with the laser focal point positioned at a depth of z=5 μm. When the focal spot is positioned inside the DT, the parasitic BJT effect is exacerbated with increasing pulse energy. This is evidenced by the fact that Q_C is roughly equal to 0.96×Q_{SX} at 11.8 nJ and increases to 1.14×Q_{SX} at 32.0 nJ. Similarly, when the focal spot is positioned outside the DT, Q_C still increases as the pulse energy is increased, however, the presence of the external n-ring shunts a significant number of electrons away from the collector. This electron shunting is evidenced by the fact that Q_C is equal to 0.71×Q_{SX} at 11.8 nJ and falls to 0.58×Q_{SX} at 32.0 nJ. Furthermore, for a focal spot positioned outside the DT, the external n-ring collects more charge than the collector, regardless of the pulse energy.

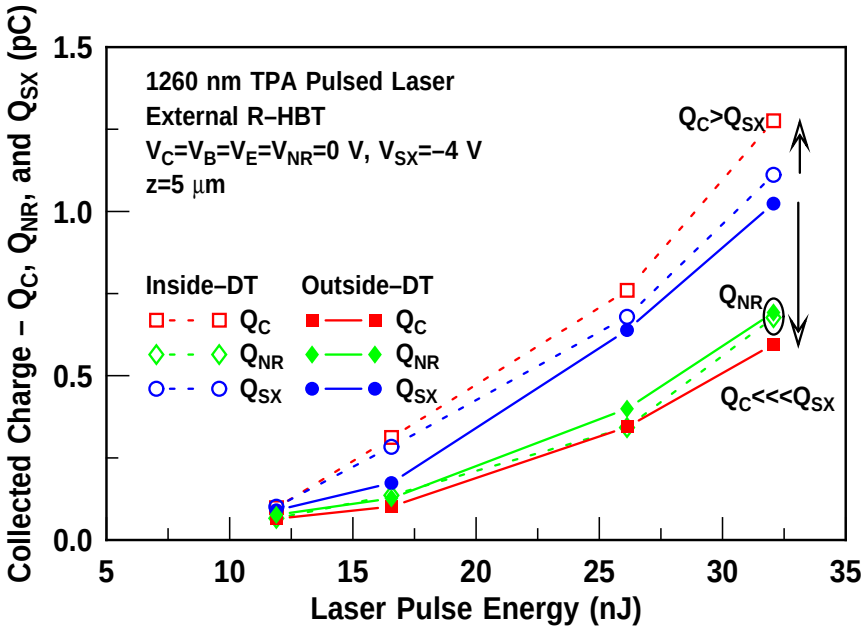

Figure 122: Q_C, Q_{NR}, and Q_{SX} vs. laser pulse energy inside and outside the DT of the external R-HBT.

In Figure 123, Q_C and Q_{SX} are re-plotted as a function of laser pulse energy using logarithmic scales for pulsed laser irradiation inside the DT. The TPA-induced excess carrier concentration (N_{2P}) is proportional to I^2, as shown in (107). Since the laser pulse energy is directly proportional to I, as shown in (104), then N_{2P} is also proportional to the square of the pulse energy. A trend line is included in this figure to capture the dependence of charge deposition on the square of the pulse energy, confirming the validity of the TPA

technique. These results suggest that the presence of the n-ring marginally increases the collector-collected charge for ion strikes inside the DT but significantly suppresses that collection for heavy ions impingent outside the DT. Moreover, these trends are amplified as the amount of charge deposition increases, which suggests that this RHBD technique may be more effective for ions with a larger LET, thereby potentially enabling a reduction in the saturation cross section for heavy ions.

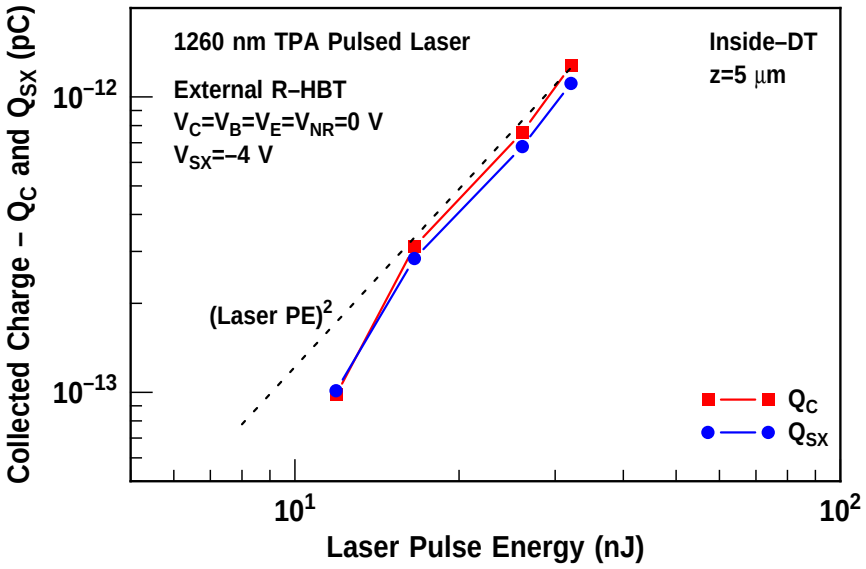

Figure 123: Logarithmic plot Q_C and Q_{SX} vs. laser pulse energy inside the DT.

8.6 Conclusion

In this chapter, the applicability of two-photon absorption to the investigation of charge collection in transistor-level layout-based RHBD variants has been verified via pulsed laser irradiation of 3rd-generation HBTs. Pulsed laser irradiation is a cheaper and less damaging experimental approach than heavy-ion microbeam irradiation. The fact that radiation-induced excess carriers are generated in proportion to I^2 allows for a deterministic 3-D mapping of the sensitive volume surrounding the transistor simply by translating it in the vertical dimension with respect to the microscope objective. The utilization of a backside irradiation technique drastically simplifies the charge-deposition dynamics since there are no dielectric or metal layers over the transistor to influence the transfer of energy into the

substrate. Moreover, unlike the SPA-induced excess carrier concentration the TPA-induced excess carrier concentration is very similar to that obtained from an energetic heavy ion. This is as a result of the fact that the TPA-induced excess carrier concentration does not decrease exponentially along the beam.

Several challenges still remain regarding the utilization of pulsed laser irradiation for probing the SEE response of SiGe HBTs. To be sure, calculations of the excess carrier concentration and pulse irradiance often neglect second-order effects such as free-carrier absorption and beam phase. Therefore, further work needs to be done in effectively correlating the pulse irradiance and pulse energy to the effective LET of a heavy ion. The results of the TPA experiments presented in this chapter agree well with the results from the heavy-ion microbeam irradiation experiments that were presented in Chapter 7. Furthermore, these TPA results provide new insights into the nature of the radiation-induced current transients on the collector, substrate, and external n-ring terminals. Current transients are also observed on the base and emitter, however, their duration is very short and the overall charge collection is dominated by the collector and substrate.

CHAPTER 9

TRANSISTOR-LEVEL RHBD APPLIED TO HBT DIGITAL LOGIC

9.1 Introduction

Candidate electronics for multi-Gbit/s space-based communications systems depend upon highly reliable and cost-effective solutions that are tolerant to atomic displacement, ionization, temperature variation, and SEEs. As shown in Chapters 3-4, SiGe HBTs are tolerant to multi-Mrad(SiO_2) ionization levels and have excellent performance at cryogenic temperatures. However, these bulk SiGe technologies are very susceptible to SEEs [191]. This SEE vulnerability stems from both the use of a lightly doped substrate and the efficient collection of heavy-ion-induced excess carriers by the base-to-collector and substrate-to-sub-collector junctions. These two phenomena often result in low threshold LETs and high saturated cross sections being measured in most bulk SiGe platforms. Moreover, at cryogenic temperatures, the increase in carrier mobility increases the sensitive volume for charge collection in these transistors, which yields even larger cross sections [13].

It is again emphasized that several recent strides have been made in the understanding and mitigation of the SEE vulnerability of HBT digital logic. Heavy-ion microbeam irradiation has been successfully used to image the localized sensitive volumes at both the transistor and circuit level [332][343]. In addition, the results from both single-photon and two-photon pulsed laser irradiation provide localized current transient information, which serves as an invaluable validation tool for 3-D TCAD simulations of ion strikes [380]. Furthermore, several circuit-level RHBD approaches have provided promising results in addressing the SEE sensitivity of HBT digital logic. To this end, recent results have demonstrated limiting cross sections, which indicate error-free operation, at LET values well above 50 MeV·cm^2/mg [350]. As previously discussed, this result was obtained by first interleaving

duplicate copies of the pass and storage cells of a standard master-slave latch to form a dual-interleaved latch, and subsequently encapsulating 16-bit shift registers configured using those latches in a TMR architecture with voting circuitry at the output. Unfortunately, this RHBD approach has significant area and power penalties. In this chapter, the SEE tolerance is investigated for 16-bit shift registers configured using standard master-slave latches with each transistor replaced with the external R-HBT, which was described in Chapters 7 and 8 [14]. This approach results in a significant reduction in the saturated cross section with a negligible power penalty and no increase in design complexity.

9.2 Experiment Details

9.2.1 16-Bit Shift Registers

SEEs in 3rd-generation HBT digital logic are investigated in this chapter using 16-bit shift registers composed of standard master-slave flip-flops configured using the CML architecture. A top-level circuit block diagram for these shift registers is illustrated in Figure 74, and the circuit schematic of the standard master-slave latch is illustrated in Figure 59. However, in the shift registers under investigation here, each transistor of the standard master-slave latch was replaced with an external R-HBT. The external R-HBTs have an A_E of 0.12×0.52 μm^2 and were configured in a single-striped CBE-layout.

The layout of the standard master-slave latch after these changes were implemented is illustrated in Figure 124, and the layout of the full 16-bit shift register is illustrated in Figure 125. The details of the latch architecture and the packaging approach are described in Chapter 6. To evaluate the implications of substrate contact spacing on the SEU response of HBT digital logic, two separate versions of the standard master-slave registers were fabricated. In the first version, a ring of substrate contacts is placed in each latch at a distance of 3 μm from the external n-ring of each external R-HBT, as shown in Figure 124. The second version is identical to the first, with the exception that the ring of substrate contacts is removed. These versions will be referred to as the *Std M/S+NR+SX* and *Std M/S+NR*, respectively.

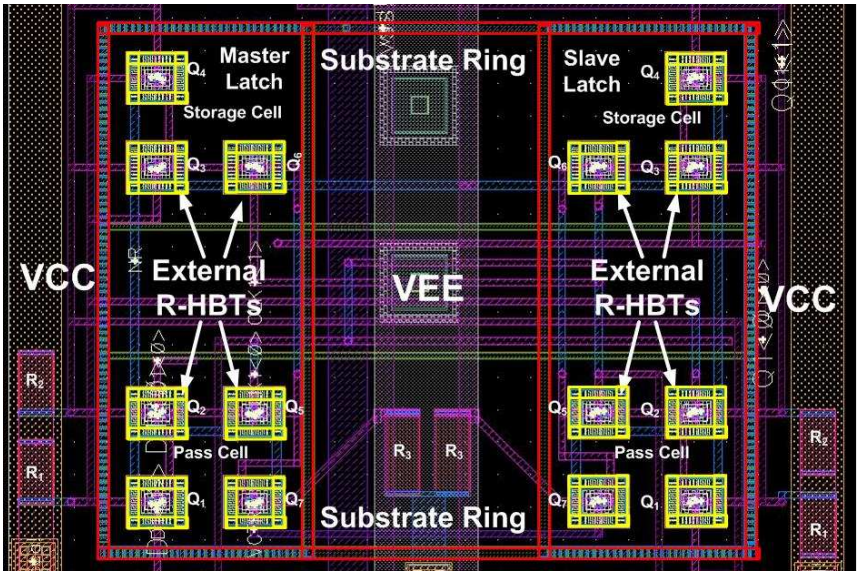

Figure 124: Layout of the Std M/S+NR+SX latch.

To benchmark the effectiveness of the transistor-level layout-based RHBD approach, the new heavy-ion broadbeam irradiation data obtained here is compared to the data for 16-bit shift registers configured using a variety of circuit-level RHBD approaches [350].

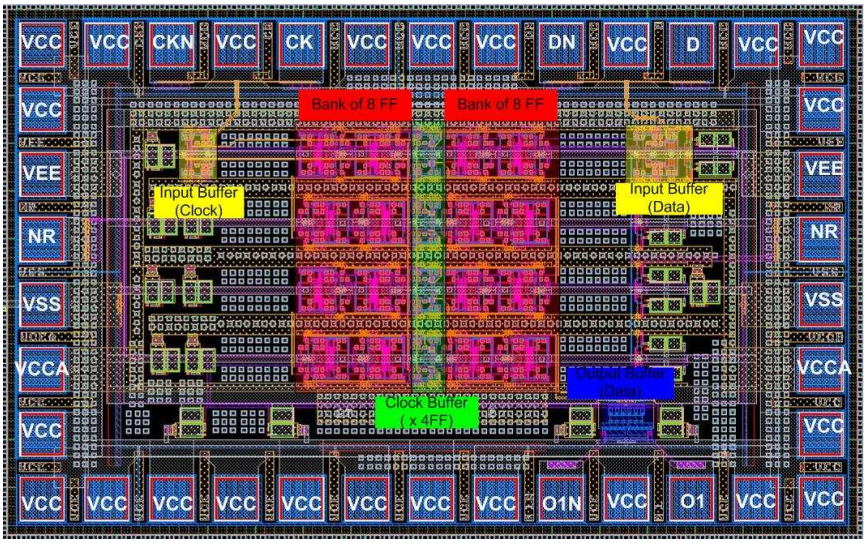

Figure 125: Layout of the Std M/S+NR+SX 16-bit shift register.

Those registers were configured using the unhardened standard master-slave latch, which utilized CBEBC-configured transistors with an A_E of 0.12×2.5 μm^2, the gated feedback

cell (GFC) latch, high- and low-power dual-interleaved (DI) latch, and TMR versions of the high-power DI and GFC registers. All of the circuit-level RHBD shift registers were constructed using CBE-configured nominal-HBTs with an A_E of 0.12×0.52 μm^2, which is the same area as the external R-HBT. The substitution of the external R-HBT for the nominal-HBT results in an 80% increase in the standard master-slave latch area, but more importantly, there is no area penalty at the circuit level and no increase in design complexity. The transistor- and circuit-level area and power consumption of the 16-bit HBT digital logic are compared in Table 10.

Table 10: Area and power consumption of circuit- and transistor-level RHBD shift registers.

Architecture	**Transistor**			**16-bit Register**	
	A_E μm^2	A_{DT} μm^2	I_{TAIL} mA	Area mm^2	Power mW
Std M/S	0.12×2.50	4.34×3.48	0.5	2.37×1.59	250
Std M/S+NR	0.12×0.52	2.72×1.50	0.5	2.37×1.59	250
Std M/S+NR+SX	0.12×0.52	2.72×1.50	0.5	2.37×1.59	250
LP-DI [340]	0.12×0.52	2.72×1.50	0.5	2.37×1.59	399
HP-DI [340]	0.12×0.52	2.72×1.50	1.0	2.37×1.59	506
HP-DI-TMR [340]	0.12×0.52	2.72×1.50	0.5	2.64×2.69	1136
HP-GFC[339]	0.12×0.52	2.72×1.50	1.0	2.37×1.59	729
LP-GFC-TMR[339]	0.12×0.52	2.72×1.50	0.5	2.64×2.69	1945

9.2.2 Heavy-Ion Broadbeam Irradiation

Heavy-ion broadbeam irradiation was performed at the TAMU facility [217] using 15 MeV/amu ^{20}Ne, ^{40}Ar, ^{84}Kr, and ^{129}Xe impingent at several angles of incidence (θ) including 0°, 45°, 60°, and 75°. Multiple die of the Std M/S+NR+SX and Std M/S+NR shift registers were packaged into a custom-designed high-speed test fixture identical to the one illustrated in Figure 75. As described in Chapter 6, BER testing was facilitated using a PRS, which was generated via the Anritsu MP1763B pulse pattern generator and was 2^7-1 bits long. Error detection and capture was performed using the Anritsu MP1764A 12.5 GHz error detector, and customized LabVIEW software was used to manage GPIB equipment, control data capture, and facilitate data analysis.

9.3 Heavy-Ion Cross Sections

9.3.1 Impact of Substrate Contact Location

The bit-error and bit-error cross sections are used to compare the heavy-ion-induced SEU response of all shift registers. For heavy ions, a plot of the cross section (σ_{HI}) as a function of LET is fitted to a Weibull distribution, which is expressed as [18][381]

$$\sigma_{HI} = \sigma_{HI\infty}\left[1 - \exp\left(\frac{-(L - L_{th})}{W}\right)^{s}\right], \tag{110}$$

where L is the heavy-ion LET, L_{th} is the threshold value of L, $\sigma_{HI\infty}$ is the saturated heavy-ion cross section, W is the scale parameter, and s is the shape parameter. From an experimental perspective, L_{th} is defined as the smallest value of L for which errors are observed, and $\sigma_{HI\infty}$ is defined as the value of σ_{HI} at which further increases in L fail to increase the number of errors observed, regardless of the heavy-ion fluence.

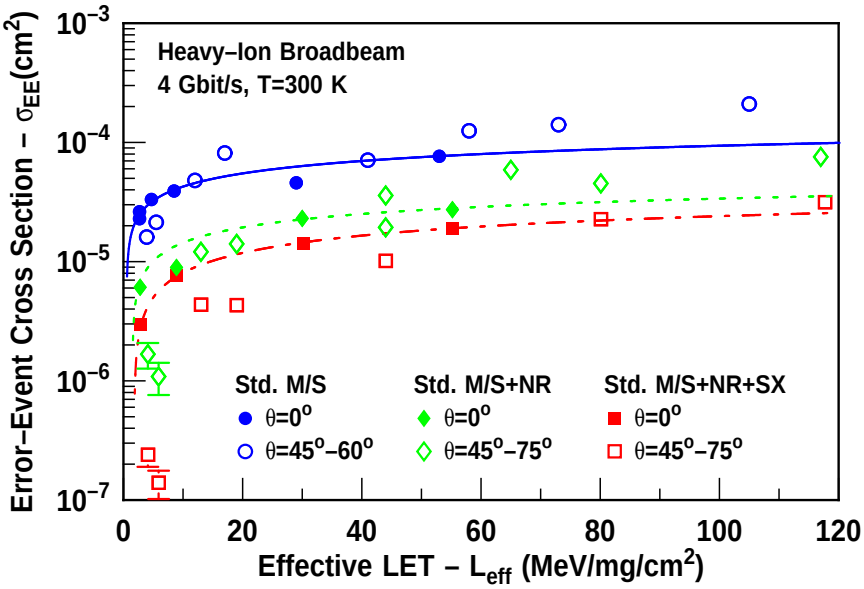

Figure 126: σ_{EE} vs. L_{eff} for the Std M/S, Std M/S+NR, and Std M/S+NR+SX shift registers at operating 4 Gbit/s.

In Figure 126, the error-event cross section (σ_{EE}) at 4 Gbit/s is plotted as a function of L_{eff} for the Std M/S, Std M/S+NR, and Std M/S+NR+SX shift registers. The closed symbols represent data from heavy ions impingent on the circuit at normal incidence (θ=0°), and open symbols represent data from heavy ions incident at θ=45°, 60°, or 75°. For heavy

ions impingent at an angle, the Weibull approximation is no longer valid, and therefore, the solid lines illustrated in Figure 126 represent a Weibull fit to the cross sections obtained from normally incident heavy ions. The Weibull parameters and corresponding goodness of fit, with 99% confidence bounds, are given in Table 11.

Table 11: Normally-incident Weibull parameters at 4 Gbit/s.

Architecture	Weibull Parameters				Goodness of Fit	
	$\sigma_{HI\infty}$ (cm^2)	L_{th}(MeV·cm^2/mg)	W	s	SSE	R^2
Std M/S	2.3×10^{-4}	0.5	500	0.4	2.93×10^{-10}	0.8454
Std M/S+NR	6.0×10^{-5}	1.5	150	0.45	2.33×10^{-11}	0.9286
Std M/S+NR+SX	4.4×10^{-5}	1.8	150	0.55	1.85×10^{-13}	0.9988

As indicated by the goodness of fit, the normally incident cross sections conform fairly well to the Weibull parameters. The replacement of the nominal-HBT with the external R-HBT, which has a significantly smaller A_E, results in a 74% reduction in the saturated σ_{EE} ($\sigma_{EE\infty}$) of the Std M/S+NR shift register and a 80% reduction for the Std M/S+NR+SX register. There corresponding changes in L_{th} are negligible.

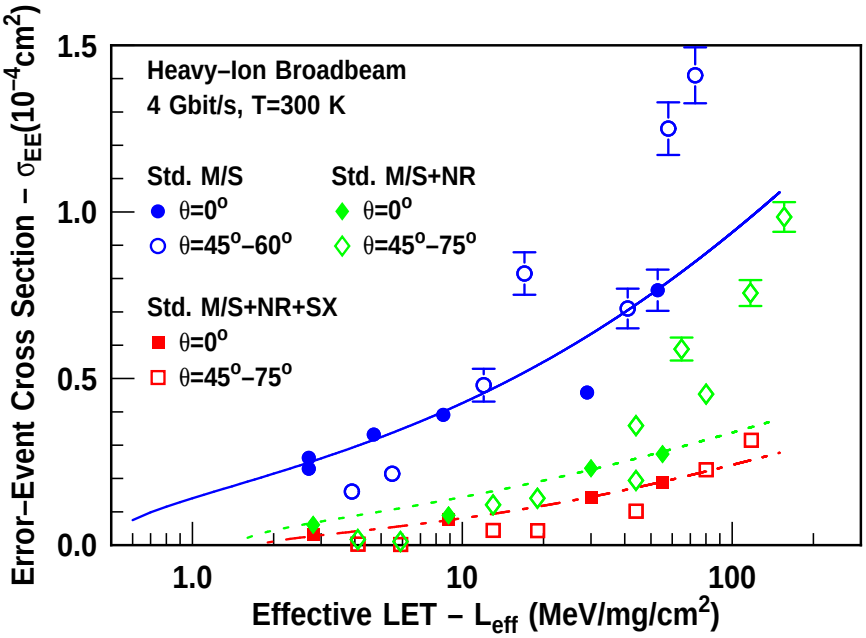

Figure 127: Figure 126 re-plotted with σ_{EE} on a linear and L_{eff} on a log scale to highlight the low LET region.

In Figure 127, σ_{EE} is plotted on a linear scale as a function of L_{eff}, which is plotted on a logarithmic scale. When illustrated in this fashion, it is easier to visualize σ_{EE} near L_{th}, and it is also evident that σ_{EE} continues to increase at the highest LETs tested. Upsets are still observed for all three registers at the lowest LET of 2.80 MeV·cm^2/mg, which was obtained using normally incident ^{22}Ne ions. The presence of upsets at these low LETs indicates that the utilization of the external R-HBT does not increase L_{th} in HBT digital logic. It should be noted, however, that even at these low LETs a 91% reduction in σ_{EE} is measured. Calculations of the on-orbit event rate in a space environment must take the particle distribution into account, and these distributions are typically heavily weighted toward the lower end, or "knee region," of the σ_{EE} vs. L_{eff} curve.

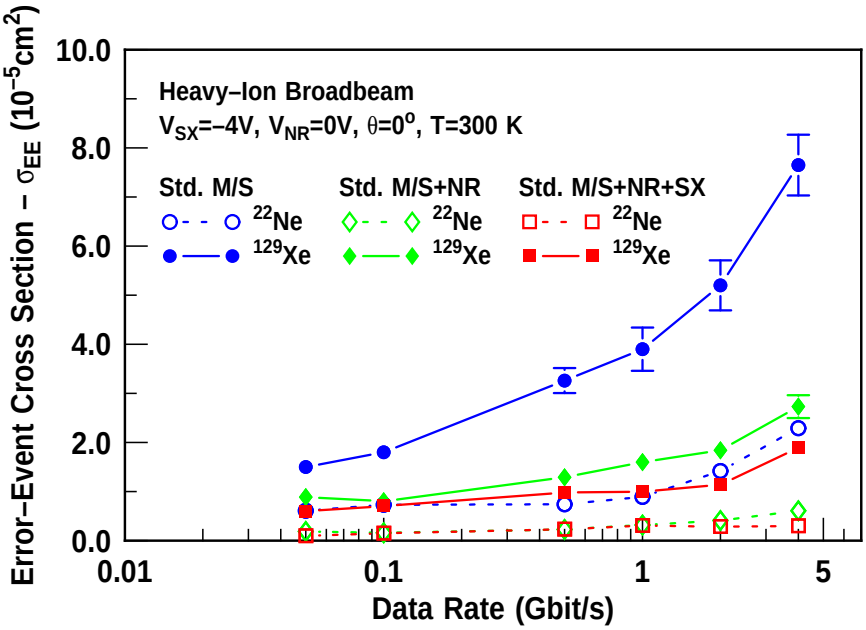

Figure 128: σ_{EE} vs. data rate for the Std M/S, Std M/S+NR, and Std M/S+NR+SX shift registers irradiated with ^{22}Ne and ^{129}Xe ions.

In Figure 128, σ_{EE} is plotted on a linear scale as a function of data rate for ^{22}Ne and ^{129}Xe irradiation of the Std M/S, Std M/S+NR, and Std M/S+NR+SX shift registers. As the data rate is increased, the clock period is reduced, and if the duration of single-event current and voltage transients remains fixed, then more bits are affected and σ_{EE} will increase. The degree of these increases is obviously heavily dependent on both the architecture of the shift register and the heavy-ion LET. Using a ^{22}Ne beam, σ_{EE} of the

Std M/S register increases by as much as 440%, as the data rate is increased from 50 Mbit/s to 4 Gbit/s. Conversely, for the Std M/S+NR and Std M/S+NR+SX registers, σ_{EE} increases by 239% and 221%, respectively. For ^{129}Xe ions, which have a higher LET, the corresponding increases are 410%, 208%, and 216% for the Std M/S, Std M/S+NR, and Std M/S+NR+SX shift registers, respectively.

As demonstrated in Chapter 6, the ratio of the cross section calculated using the number of bit errors to cross section calculated using the number of error events $\left(\frac{\sigma_{BE}}{\sigma_{EE}}\right)$ is a good indicator of the error signature composition. In Figure 129, $\frac{\sigma_{BE}}{\sigma_{EE}}$ is plotted as a function of data rate for ^{22}Ne and ^{129}Xe irradiation of the Std M/S, Std M/S+NR and Std M/S+NR+SX, shift registers.

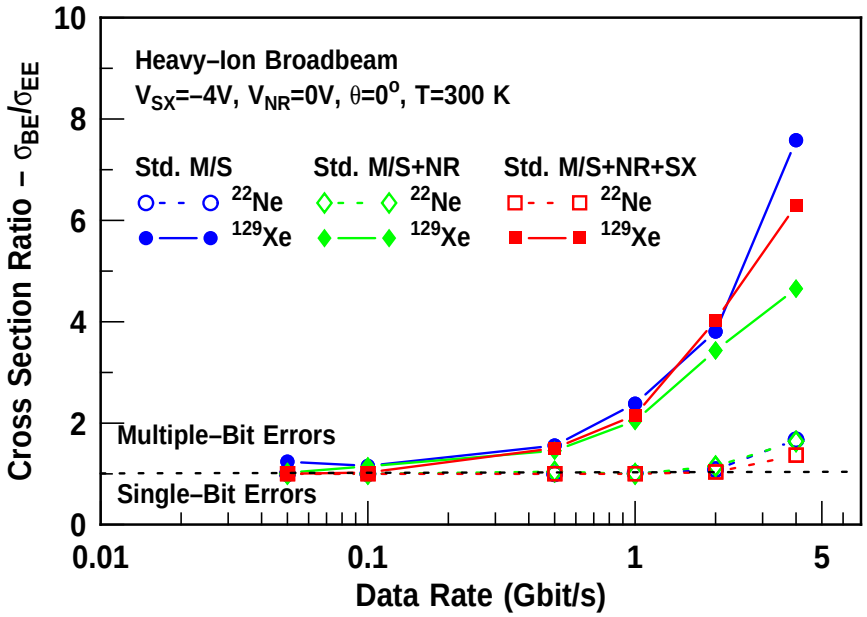

Figure 129: $\frac{\sigma_{BE}}{\sigma_{EE}}$ vs. data rate for the Std M/S, Std M/S+NR, and Std M/S+NR+SX shift registers irradiated with ^{22}Ne and ^{129}Xe ions.

Single-bit errors dominate the SEU response for all three shift registers during ^{22}Ne irradiation up to a data rate of 2 Gbit/s, as evidenced by the fact that $\frac{\sigma_{BE}}{\sigma_{EE}} \approx 1$ across this range of data rates. Beyond 2 Gbit/s, $\frac{\sigma_{BE}}{\sigma_{EE}}$ increases by almost 200%, which indicates the presence of multiple-bit errors in the upsets. Not surprisingly, when ^{129}Xe ions are used, $\frac{\sigma_{BE}}{\sigma_{EE}} \ggg 1$ from data rates as low as 500 Mbit/s, and for the Std M/S register, $\frac{\sigma_{BE}}{\sigma_{EE}}$ increases by over 6X as the data rate is increased to 4 Gbit/s. At this high LET and data rate,

the corresponding increases for the Std M/S+NR and Std M/S+NR+SX shift registers are 500% and 400%, respecitively. Clearly, the Std M/S+NR and Std M/S+NR+SX registers offer some degree of SEE mitigation over the range of heavy-ion LETs and data rates tested. These benefits are derived from a combination of using single-striped CBE-configured HBTs to reduce A_{DT}, and the implementation of the external n-ring to suppress charge collection for heavy ions impingent outside the DT.

9.3.2 Impact of the Angle of Incidence

At most heavy-ion broadbeam facilities, it takes a longer time to change the ion species than to change the angle of the stage with respect to the ion beam. Therefore, to optimize beam time, irradiation at a non-zero angle of incidence is used to increase the number of LET values by plotting the L_{eff} (101) on the x-axes of Figures 126 and 127. As previously indicated, the open and closed symbols in Figure 126 are used to represent heavy ions impingent on the shift register at normal incidence and at an angle, respectively. Upon close inspection of Figure 126, for ^{22}Ne ions that are below the knee of the Weibull fit, σ_{EE} decreases as L_{eff} is increased. Conversely, for ^{129}Xe ions that are closer to $\sigma_{EE\infty}$, σ_{EE} increases with increasing L_{eff}. These trends are also observed for the bit-error cross section (σ_{BE}).

In Figure 130, σ_{EE} is plotted as a function of θ for ^{22}Ne and ^{129}Xe irradiation of the Std M/S, Std M/S+NR, and Std M/S+NR+SX shift registers operating at 4 Gbit/s. As θ is increased from 0° to 60° during ^{22}Ne irradiation, σ_{EE} decreases by only 6.5% for the Std M/S register; however, the corresponding decreases for the Std M/S+NR and Std M/S+NR+SX registers are 82% and 93%, respectively. Conversely, as θ is increased from 0° to 60° during ^{129}Xe irradiation, σ_{EE} increases by as much as 174% for the Std M/S register, while the corresponding increases for the Std M/S+NR and Std M/S+NR+SX registers are 176% and 66%, respectively.

Heavy ions that are incident at grazing angles, which are defined as $\theta \ggg 45^{\circ}$, have been traditionally observed to increase the upset rates in many CMOS platforms. This result has been attributed to the fact that heavy ions impingent at non-zero angles of incidence

have a much stronger lateral component and deposit more charge closer to the topside Si surface. Furthermore, for a high density of MOSFETs multiple nodes may be affected at once, which can cause MBUs. Conversely, in an HBT environment, foundry design rules mandate a much larger spacing between transistors, and the presence of the DT perturbs the heavy-ion charge track. Therefore, at low LETs and large grazing angles, the amount of charge deposited close to the surface may not be much greater than at normal incidence, which would explain the lack of variation in σ_{EE} as a function θ for the Std M/S shift register. At higher LETs, significantly more charge is deposited closer to the topside Si surface, which explains the increases in σ_{EE} as a function of θ observed for the Std M/S register during ^{129}Xe irradiation. However, it should also be noted that at grazing angles of incidence, the increased charge deposition at higher LETs may be compensated for by the fact that the ion range is inversely proportional to LET.

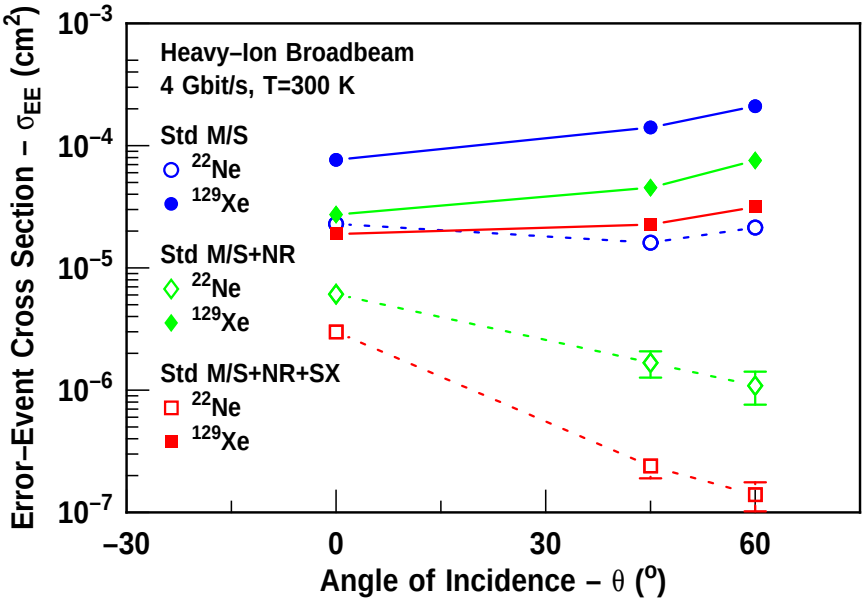

Figure 130: σ_{EE} vs. θ for the Std M/S, Std M/S+NR, and Std M/S+NR+SX shift registers operating at 4 Gbit/s and irradiated with ^{22}Ne and ^{129}Xe ions.

In Figure 131, $\frac{\sigma_{BE}}{\sigma_{EE}}$ is plotted as a function of θ for ^{22}Ne and ^{129}Xe irradiation of the Std M/S, Std M/S+NR, and Std M/S+NR+SX shift registers operating at 4 Gbit/s. At 4 Gbit/s, multiple-bit errors are observed for all registers both at θ=0° and 60° and even at LETs of 2.80 MeV·cm^2/mg. As evidenced by the variation in $\frac{\sigma_{BE}}{\sigma_{EE}}$ as a function of LET,

when L_0 is increased, longer error events are observed for normally incident ion strikes than for heavy ions impingent at θ=60°. This decrease in $\frac{\sigma_{BE}}{\sigma_{EE}}$ as θ is increased is indicative of charge sharing phenomena among multiple transistors. Multiple-bit errors can be caused either by a robust upset emanating from a single transistor or by several less robust upsets emanating from several transistors. For a normally incident heavy ion, it is more likely that a single transistor collects most of the heavy-ion-induced excess carriers because the charge track has a stronger vertical component. Conversely, at large angles of incidence, a single heavy ion has a much stronger lateral component, and the excess carriers may be distributed among several transistors. In the latter case, it is more likely that the upsets emanating from each transistor are not as robust as for a normally incident heavy ion, which would lead to a larger number of single-bit errors and a corresponding reduction in $\frac{\sigma_{BE}}{\sigma_{EE}}$ as θ is increased.

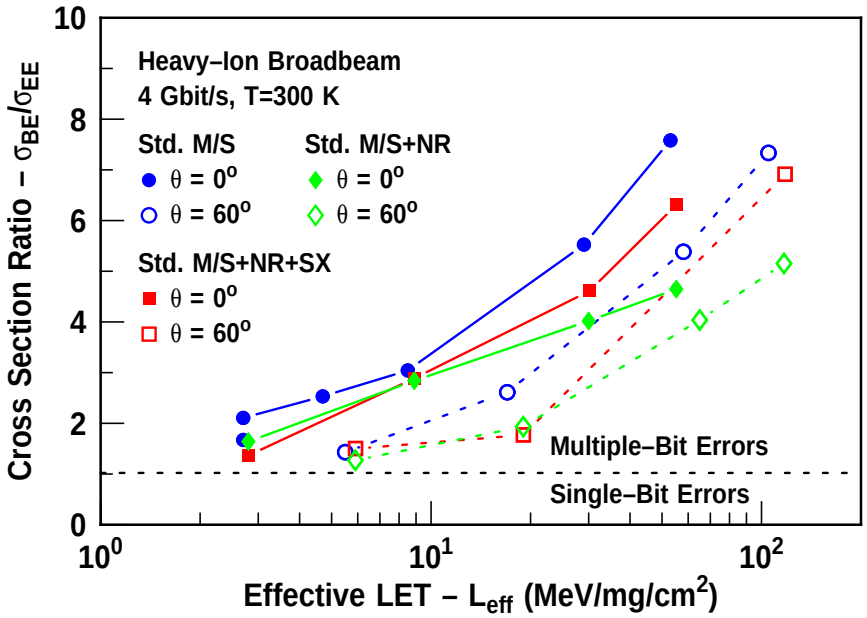

Figure 131: $\frac{\sigma_{BE}}{\sigma_{EE}}$ vs. θ for the Std M/S, Std M/S+NR, and Std M/S+NR+SX shift registers operating at 4 Gbit/s and irradiated with ^{22}Ne and ^{129}Xe ions.

9.3.3 Impact of the Substrate and N-ring Voltage

When negative voltage rails are used with CML, the substrate terminal is typically biased at the lowest voltage to suppress noise. For these 16-bit shift registers, the substrate

node is typically held at -4 V, which keeps the substrate-to-sub-collector junction reverse biased and is the source of heavy-ion-induced SEEs. In Figure 132, σ_{EE} is plotted as a function of L_{th} for heavy-ion broadbeam irradiation of the Std M/S, Std M/S+NR, and Std M/S+NR+SX registers operating at 4 Gbit/s and at V_{NR}=-4 V and -6 V. As V_{SX} is reduced from -4 V to -6 V, there is little change in σ_{EE} for both the Std M/S+NR and Std M/S+NR+SX shift registers across all LETs, which indicates that a change of just -2 V in V_{SX} is too small for the heavy-ion-induced potential modulation to have an impact on the circuit-level response.

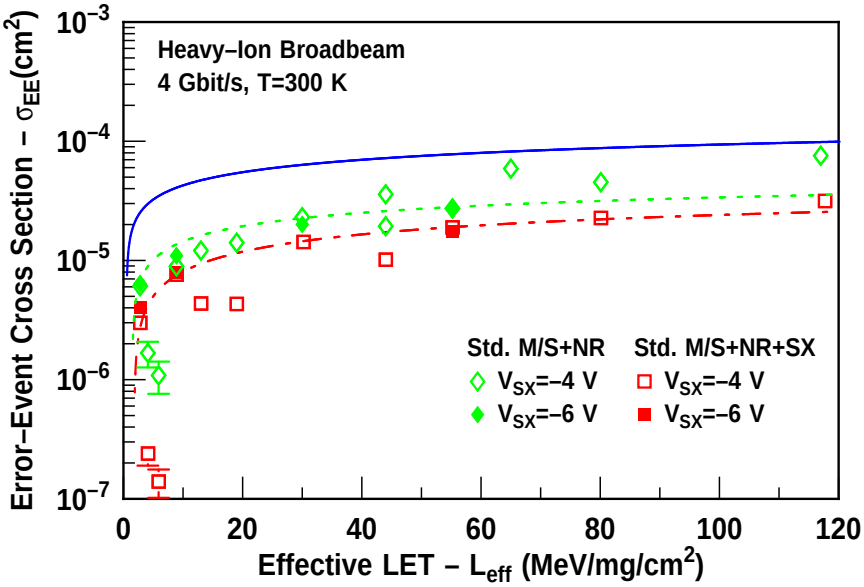

Figure 132: V_{SX} dependence of σ_{EE} vs. L_{eff} for the Std M/S, Std M/S+NR, and Std M/S+NR+SX shift registers operating at 4 Gbit/s.

In Figure 133, σ_{EE} is plotted as a function of L_{eff} for heavy-ion broadbeam irradiation of the Std M/S, Std M/S+NR, and Std M/S+NR+SX shift registers at 4 Gbit/s and at V_{NR}=0 V and 4 V. Regardless of the heavy-ion LET or data rate, σ_{EE} increases as V_{NR} is increased from 0 V to 3 V. This circuit-level heavy-ion broadbeam result contradicts the findings from transistor-level heavy-ion microbeam and pulsed laser irradiation, which indicate that the collector-collected charge decreases as V_{NR} is increased.

In Figure 134, σ_{EE} is plotted as a function of the n-ring-to-substrate voltage (V_{NRSX}) for the Std M/S+NR and Std M/S+NR+SX shift registers operating at 1 Gbit/s during ^{84}Kr

irradiation. In Chapter 7, it is shown that increasing V_{NR} from 0 V to 4 V for the external R-HBT yields a 28.9% reduction in $Q_{C,INT}$, which can be attributed to the suppression of collector-collected charge for heavy ions impingent outside the DT.

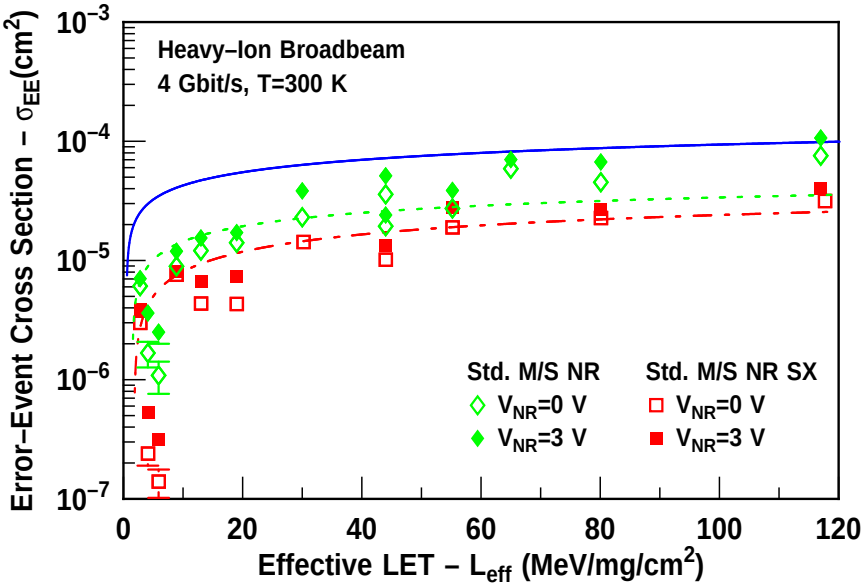

Figure 133: V_{NR} dependence of σ_{EE} vs. L_{eff} for the Std M/S, Std M/S+NR, and Std M/S+NR+SX shift registers operating at 4 Gbit/s.

However, as shown in Figure 134, σ_{EE} is observed to increase as V_{NRSX} is increased. Moreover, this behavior exhibits a strong dependence on substrate contact location. As illustrated in Figure 125, both versions of the shift register employ peripheral substrate contacts just inside the pad frame of the chip. However, for the Std M/S+NR+SX register, rings substrate contact rings are placed inside each latch and the local electric fields associated with the substrate-to-n-ring junction are much stronger when compared to the Std M/S+NR register. Therefore, for a stronger substrate-to-n-ring electric field, the collection of electrons by the n-ring is increased and σ_{EE} is consistently lower for the Std M/S+NR+SX register than for the Std M/S+NR register.

Increasing the electric field in bulk SiO_2 has been shown to increase charge yield by suppressing carrier recombination. As the electric field is increased in bulk Si, heavy-ion-induced excess carriers are also less likely to recombine, and the amount of electrons available for collection by the n-ring and sub-collector of each transistor also increases.

Therefore, as V_{NRSX} is increased past 5 V, significant increases in σ_{EE} are observed for the Std M/S+NR register. Placing substrate rings close to the external n-ring, as in the case of the Std M/S+NR+SX register, suppresses these effects.

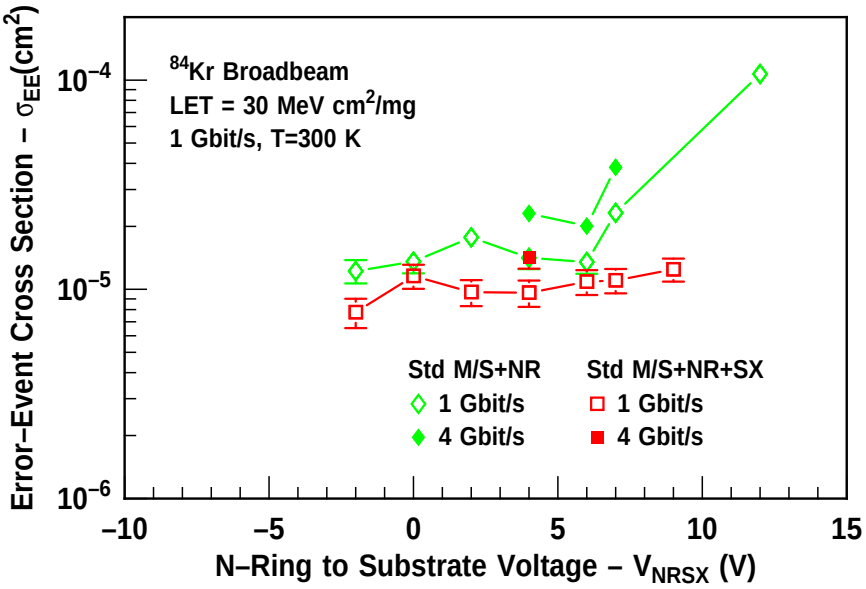

Figure 134: σ_{EE} vs. V_{NRSX} of the Std M/S+NR and Std M/S+NR+SX shift registers operating at 1 Gbit/s and 4 Gbit/s and irradiated with ^{84}Kr ions.

9.3.4 Comparison of Transistor- and Circuit-Level RHBD Approaches

As evidenced by the reductions in the laser-induced average BIE presented in Chapter 5, several circuit-level RHBD techniques are reasonably effective at SEE mitigation for HBT digital logic. Furthermore, in Chapter 6, the interleaving of duplicate copies of the standard master-slave latch was found to be effective at reducing the medium-energy proton-induced cross sections at both 300 K and 77 K. In this section, the heavy-ion cross sections for a variety of circuit-level RHBD techniques are compared to the cross sections obtained using the transistor-level layout-based RHBD technique introduced in Chapter 7. The circuit-level broadbeam data has been previously published in [350].

The Weibull and goodness-of-fit parameters of both the transistor- and circuit-level RHBD techniques for normally-incident ions at 1 Gbit/s are given in Table 12. As was observed for the 4 Gbit/s data shown in Table 11, at 1 Gbit/s there are non-negligible reductions in $\sigma_{EE\infty}$ but no impact on L_{th}. At 1 Gbit/s, the implementation of the external

n-ring and the reduction of A_E result in reductions of 63% and 89% in $\sigma_{EE\infty}$ for the Std M/S+NR and Std M/S+NR+SX registers, respectively. The utilization of the LP DI, HP DI, HP DI TMR, and GFC circuit-level RHBD registers results in reductions in $\sigma_{EE\infty}$ of 75%, 84%, 94%, and 76%, respectively.

Table 12: Normally-incident Weibull parameters at 1 Gbit/s.

Architecture	Weibull Parameters				Goodness of Fit	
	$\sigma_{EE\infty}$ (cm^2)	L_{th}(MeV·cm^2/mg)	W	s	SSE	R^2
Std M/S	5.5×10^{-5}	2.0	100	0.32	1.583×10^{-11}	0.9009
Std M/S+NR	3.5×10^{-5}	2.0	150	0.45	4.76×10^{-13}	0.9945
Std M/S+NR+SX	1.0×10^{-5}	2.5	10	1.2	2.06×10^{-13}	0.9959
LP DI	2.4×10^{-5}	2.0	120	0.4	6.12×10^{-13}	0.9868
HP DI	1.5×10^{-5}	2.0	20	1.4	7.80×10^{-12}	0.9406
HP DI TMR	5.5×10^{-6}	2.0	120	1.0	1.12×10^{-14}	0.9938
GFC	2.3×10^{-5}	3.0	120	1.0	5.56×10^{-13}	0.9788

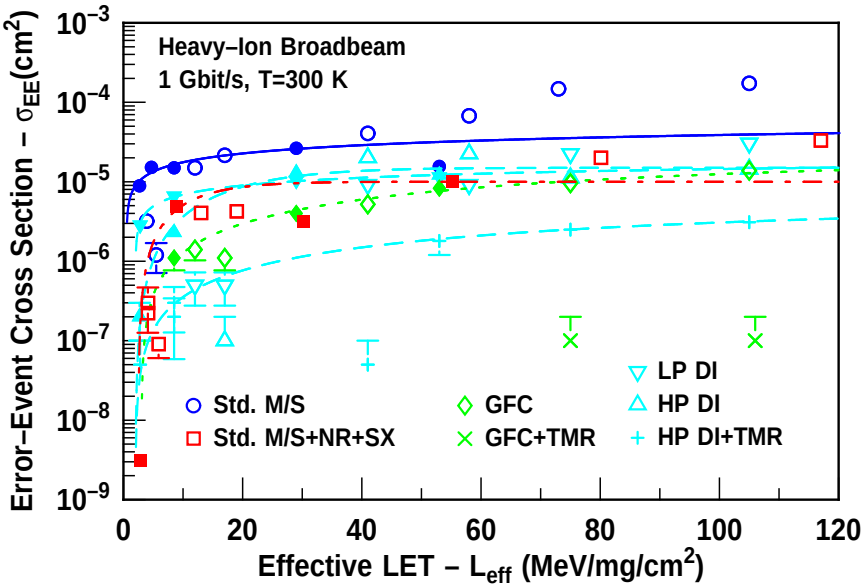

Figure 135: Comparison of σ_{EE} vs. L_{eff} for all transistor- and circuit-level RHBD techniques.

In Figure 135, σ_{EE} is plotted as a function of effective LET at 1 Gbit/s for all of the circuit-level RHBD approaches defined in Table 10. The reduction in $\sigma_{EE\infty}$ for the Std M/S+NR+SX register is comparable to that of the LP DI, HP DI, and GFC. In Figure 136, σ_{EE} is plotted as a function of power dissipation for ^{129}Xe irradiation at 1 Gbit/s for the transistor- and circuit-level RHBD approaches defined in Table 10. The Std M/S+NR+SX

shift register provides as much mitigation as the non-TMR circuit-level RHBD approaches at only a fraction of the power dissipation. To be sure, the power dissipated by the Std M/S+NR+SX register is only 35% that of the GFC, 55% that of the LP DI, and 49% that of the HP DI. The application of TMR encapsulation to the HP DI shift register still outperforms all other RHBD approaches but requires 5.2X more power, while the power penalty for the Std M/S+NR+SX shift register is only 1.15X.

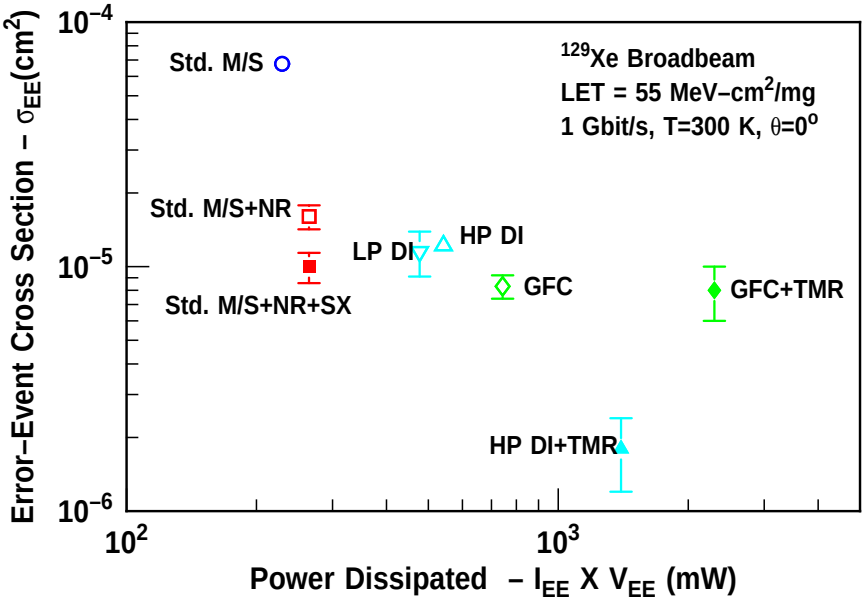

Figure 136: σ_{EE} vs. P_{diss} of all transistor- and circuit-level RHBD techniques.

9.3.5 Impact of Transistor Geometry

As shown in Table 10, the latches of the Std M/S shift register were designed using multiple-striped CBEBC-configured transistors, each with an A_E of 0.12×2.5 μm^2. Although there have been no comprehensive studies of the impact of transistor geometry on heavy-ion cross sections in HBT digital logic, it is widely accepted that increasing A_E necessarily increases A_{DT}, which has been shown to enhance the collector-collected charge for heavy ions impingent inside the DT. Although a determination of the circuit-level sensitive area in a heavy-ion broadbeam environment is still to be determined, to first order, it can still be approximated by comparing various "presumed" sensitive areas with the measured σ_{EE} and σ_{BE}.

The area enclosed within the DT, the area bounded by the DT, and the rectangular area 1μm and 5μm outside the DT for CBE- and CBEBC-configured transistors with an A_E of 0.12×0.52, 0.12×2.00, and 0.12×2.50 μm^2 are given in Table 13.

Table 13: A comparison of several transistor-level sensitive areas.

Sensitive Area	Emitter (μm^2)	Inside DT (μm^2)	Outside DT (μm^2)	Outside DT + 1μm (μm^2)	Outside DT + 5μm (μm^2)
CBE	0.12×0.52	1.50×2.72	3.58×4.80	5.58×6.80	13.58×14.80
Single Stripe	0.0624	4.08	17.184	37.944	200.964
CBE	0.12×2.00	2.98×2.72	5.06×4.80	7.06×6.80	15.06×14.80
Single Stripe	0.24	8.1056	24.288	48.008	222.888
CBEBC	0.12×2.50	3.48×4.34	5.56×6.42	7.56×8.42	15.56×16.42
Multiple Stripe	0.3	15.103	35.695	63.655	255.495

In Chapter 5, it was demonstrated that there is significant variation in the upset rate for HBT digital logic, both at the circuit-block level and among the transistors within in a given circuit block. In a heavy-ion broadbeam environment, the upset rate is determined by the combined sensitivity of all transistors in the register. Moreover, for a given fluence, only those ions that are impingent on the sensitive area of the shift register generate upsets. Therefore, σ_{EE} is representative of the cumulative "sensitive area" of the circuit.

In Figure 137, σ_{EE} is plotted as a function of L_{eff} for the Std M/S shift register at 50 Mbit/s, 1 Gbit/s, and 4 Gbit/s. Also indicated on this plot are the theoretical sensitive areas, which are calculated based on the summations of the transistor-level sensitive areas in Table 13. Several observations can be made from Figure 137. First, for ^{129}Xe ions impingent at non-zero angles of incidence and at data rates of 1 Gbit/s and 4 Gbit/s, σ_{EE} is consistently larger than the theoretical cross section, provided that only the area enclosed within the DT is considered for charge collection. Second, if it is assumed that the sensitive area for charge collection extends at least up to 1 μm outside the DT and that all transistors are equally sensitive, then this theoretical cross section consistently overestimates the measured $\sigma_{EE\infty}$. Therefore, to account for the difference in A_E of the transistors used in the latches of the Std M/S and Std M/S+NR shift registers, the theoretical cross section is computed using the cumulative A_{DT} (ΣA_{DT}) for all transistors in the shift register.

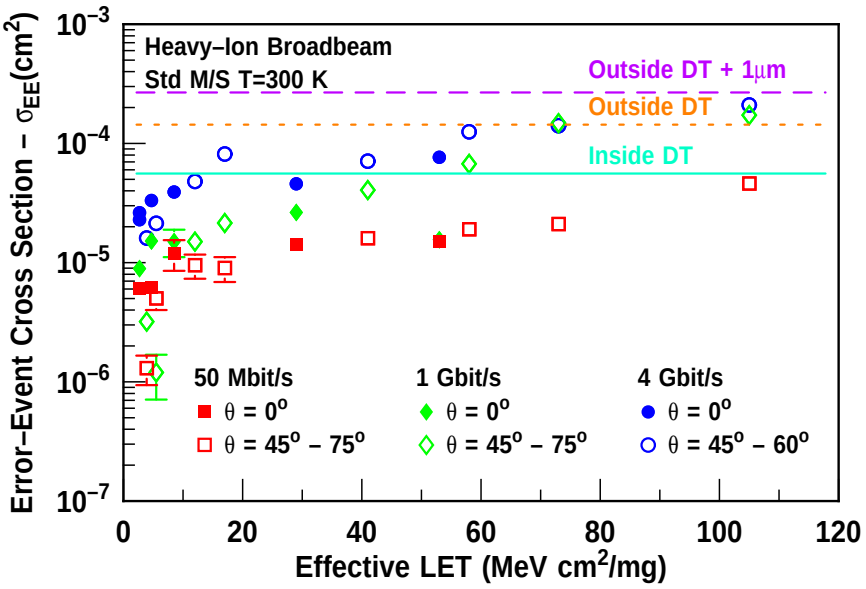

Figure 137: Comparison of several theoretical sensitive areas and measured σ_{EE} vs. L_{eff} for the Std M/S shift register.

The error-event cross section is normalized to the cumulative A_{DT} $\left(\frac{\sigma_{EE}}{\Sigma A_{DT}}\right)$ and plotted on a logarithmic scale as a function of linear L_{eff} in Figure 138 and on a linear scale as a function of logarithmic L_{eff} in Figure 139.

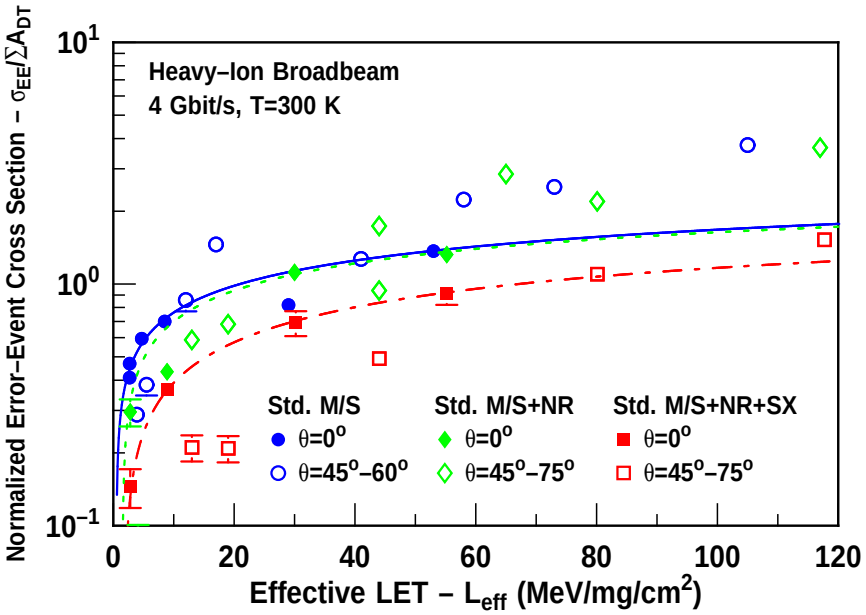

Figure 138: Normalized σ_{EE} vs. L_{eff} for the Std M/S, Std M/S+NR, and Std M/S+NR+SX shift registers at 4 Gbit/s.

The summation of the area enclosed within the DT for all transistors in the shift register is 5.59×10^{-5} cm^2 for the Std M/S shift register and 2.05×10^{-5} cm^2 for both the Std M/S+NR and Std M/S+NR+SX shift registers. At LETs below 30 MeV·cm^2/mg, a significant reduction in $\frac{\sigma_{EE}}{\Sigma A_{DT}}$ is observed for both the Std M/S+NR and Std M/S+NR+SX shift registers. As the LET is increased, the $\frac{\sigma_{EE\infty}}{\Sigma A_{DT}}$ of the Std M/S+NR shift register is equal to that of the Std M/S shift register at both normal and non-normal angles of incidence. After the difference in transistor geometry is accounted for, $\frac{\sigma_{EE}}{\Sigma A_{DT}}$ is still reduced by up to 24% when the external n-ring is used in conjunction with substrate contact rings in the latches.

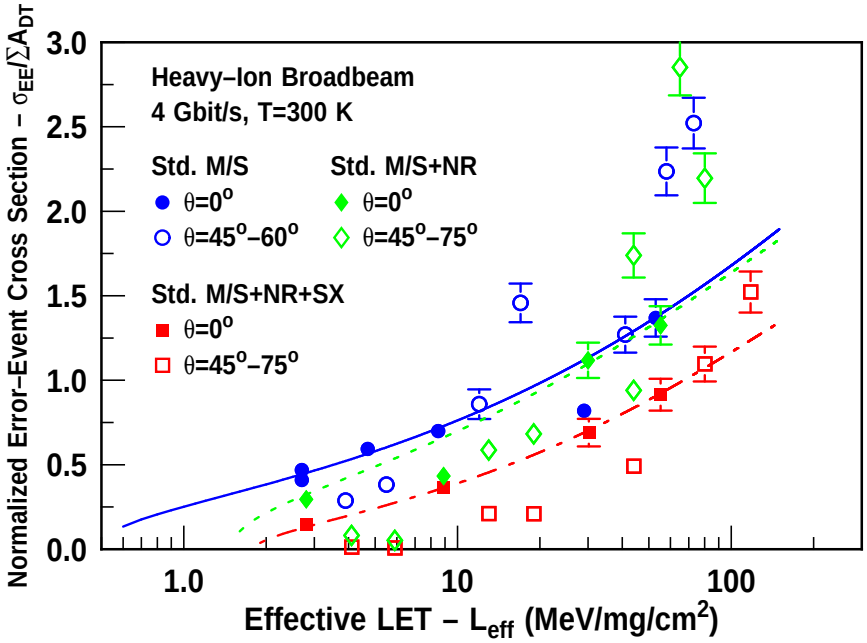

Figure 139: Figure 138 re-plotted on a linear-log scale.

9.4 On-Orbit Event Rate Calculations

The σ_{EE} vs. L_{eff} curves presented in this chapter are the penultimate step in the evaluation of the efficacy of these transistor-level layout-based RHBD approaches. Most importantly, the metric that is of interest to system designers and mission planners is the on-orbit event rate, which is a measure of the error activity that can be expected for a given circuit in a given space environment. To be sure, there are several ways to calculate this error rate. These include the traditional RPP calculation using the integral

of the Weibull curve and the CRIER or SPACERAD code, the effective flux approach, the redistributed flux approach, the low-LET approach, the shape dependent approach, the LET flux×cross section approach, and the SEU figure of merit approach [381]. The SEU figure of merit approach is used to analyze the data sets in this chapter. Descriptions of the other techniques for on-orbit error rate calculations are provided in [381], and it is noted that most of these methods are very complicated and usually require much more information than is available here.

As described in Chapter 6, in the SEU figure of merit approach is based on the calculation of the product of the on-orbit rate coefficient (C) and the SEU FOM. This product is equivalent to the upset rate in units of upsets/bit/day [349]. The SEU FOM is calculated as

$$FOM = \frac{\sigma_{EE\infty}}{L_{0.25}^2}, \tag{111}$$

where $L_{0.25}$ is the value of the L_{eff} at σ_{EE}=0.25×$\sigma_{EE\infty}$ and can be written as

$$L_{0.25} = L_{th} + \left(W \times 0.288^{\frac{1}{s}}\right), \tag{112}$$

where W is the Weibull scale parameter and s is the Weibull shape parameter. Depending on the specific value of C for a given orbit, the upset rate (R) is then written as

$$R = C \times FOM. \tag{113}$$

To facilitate the computation of the on-orbit event rate, an Adams 90% environment for geosynchronous satellite orbit will be assumed, which invokes the value of 500 for C [381]. This environment is particularly useful for estimating the peak instantaneous intensity of cosmic rays during a mission and is a conservative estimate of the activity encountered on longer missions. Using this value of C and the relationships for FOM and $L_{0.25}$ given in (111) and (112), the corresponding upset rates for several shift registers are calculated in Table 14.

There is an increase of just under 1000X when the value of R computed for the Std M/S register is compared to the value computed for the HP DI TMR register, which has the lowest error rate of all the hardening techniques. Furthermore, all of the circuit-level

Table 14: On-orbit event rate calculations at 1 Gbit/s.

Architecture	**Upset Rate Parameters**			
	$\sigma_{HI\infty}$ (cm^2)	$L_{0.25}$(MeV·cm^2/mg)	FOM	R
Std M/S	5.5×10^{-5}	4.04	3.36×10^{-6}	1.68×10^{-3}
Std M/S+NR	$\mathbf{3.5\times10^{-5}}$	**9.43**	$\mathbf{3.93\times10^{-7}}$	$\mathbf{1.96\times10^{-4}}$
Std M/S+NR+SX	$\mathbf{1.0\times10^{-5}}$	**6.04**	$\mathbf{2.74\times10^{-7}}$	$\mathbf{1.37\times10^{-4}}$
LP DI	2.4×10^{-5}	7.34	4.45×10^{-7}	2.23×10^{-4}
HP DI	1.5×10^{-5}	10.22	1.44×10^{-7}	7.18×10^{-5}
HP DI TMR	5.5×10^{-6}	36.06	4.11×10^{-9}	2.06×10^{-6}
GFC	2.3×10^{-5}	37.56	1.63×10^{-8}	8.16×10^{-6}

RHBD techniques are significantly more tolerant than the transistor-level layout-based approaches, albeit at an increased transistor count, circuit area, and power dissipation. Said another way, a 10X advantage can be gained in the on-orbit event rate with minimal area or power penalty by just reducing A_{DT}, including the external n-ring, and implementing close substrate contacts. These results indicate that although there is some benefit in the utilization transistor-level layout-based RHBD techniques, they are by no means a standalone solution for SEE mitigation in high-speed HBT digital logic. However, they can be used in conjunction with other circuit- and system-level hardening approaches towards achieving this goal.

It should also be noted that there are several assumptions in these calculations that degrade the accuracy of the value calculated for R. First, although the Weibull fit is quite good, only normally incident data was used in determining those parameters. As stated before, heavy ions incident at non-normal angles of incidence are not well captured by the Weibull function, and when these values are removed, several valid L_{eff} points are expunged, which degrades the validity of the fit. Second, the modification of L_{eff} by funneling effects was not taken into account. Funneling processes extend the heavy-ion charge track past the depletion region and increase the L_{eff}, as described in [382]. Third, modifications to the "true RPP" shape that affect the cross section measured at large angles of incidence as a function of L_{eff} were also not taken into account. Finally, it should be emphasized that there is often no unique four-parameter Weibull fit to most σ_{EE} vs. L_{eff} data. In fact, very good non-linear least square regression fits, with $R^2 \ggg 0.99$, can be obtained by using

quite a wide range of W and $\sigma_{EE\infty}$ values, as demonstrated in [383]. In several situations it has been recommended that the scale parameter, W, be restricted to values not greater than 100 [384]. In this chapter, the fitting procedure focused on alterations of L_{th} and σ_{EE}, and changes to W and s were minimized as much as possible. Despite the challenges involved in calculating an accurate on-orbit event rate, the results do indicate, with a high degree of confidence, that the layout-based transistor-level RHBD approach combined with utilization of minimum-geometry transistors, will yield reduced upset rates for HBT digital logic in space-based environments.

9.5 Conclusion

These results clearly indicate that the transistor-level layout-based RHBD approach presented here should be considered a viable tool in for SEE mitigation in circuits utilizing SiGe HBTs in a radiation-rich environment. Demonstrated here for multi-Gbit/s HBT digital logic in the 3$^{\text{rd}}$-generation platform, this approach can be readily adapted to analog, RF, and mixed-signal circuits with little performance penalty, across all existing SiGe technology platforms. Careful analysis of sensitive transistor nodes and optimal layout practices can be used to minimize the overall circuit area penalty. The level of SEU immunity afforded will depend on several factors including the doping and substrate resistivity, critical charge, bias, data rate, radiation particle type, and heavy-ion LET. Further reduction in the error-event cross section may be achieved by combining transistor-level and circuit-level RHBD techniques and should be addressed within the context of the CML-based latch architectures explored here.

CHAPTER 10

CONCLUSIONS AND RECOMMENDATIONS

In this thesis, the total-dose and single-event response of 1st- through 4th-generation HBTs has been investigated using a combination of 3-D TCAD, variable-energy protons, 1.2 MeV ^{60}Co gammas, 10 keV x-rays, 1 MeV neutrons, single-photon and two-photon pulsed laser irradiation, heavy-ion microbeam, and heavy-ion broadbeam irradiation. The results from both simulation and experimental testing indicate that although SiGe HBTs are remarkably tolerant to multi-Mrad(SiO_2) ionization levels, single-event effects continue to present challenges to the utilization of this technology in extreme environments.

10.1 Total-Dose Effects

The multi-Mrad(SiO_2) radiation tolerance of SiGe HBTs is several orders of magnitude greater than the 130 krad(SiO_2) levels that would be expected in a typical lunar mission. Moreover, as demonstrated in Chapter 3 using the results from medium-energy proton irradiation, the total-dose tolerance of this technology is heavily dependent on the location of the Si/SiO_2 interfaces in relation to the BE and BC depletion regions. This effectively means that subtle changes in the transistor layout as the technology is scaled can have a significant impact on the observed tolerance, as is evidenced by the significant reduction in the radiation-induced excess base current observed in going from the 1st- to the 3rd-generation technology platform. Degradation of the *ac* performance characteristics is negligible up to 6 Mrad($Si)_2$), and when compared to CMOS platforms, there is minimal increase in the radiation-induced degradation as a function of transistor bias. High-temperature annealing significantly reduces the post-irradiation excess base current.

Most radiation-rich environments are composed of a wide spectrum of particle types, energies, flux, and ambient temperature. To this end, ground-based irradiation performed using multi-energetic protons, 1.2 MeV ^{60}Co gammas, 10 keV x-rays, and 1 MeV neutrons has

been used to investigate the effects of dose rate, flux, and radiation source on the excess base current. The transistor response is determined by a combination of the energy-dependent particle LET and technology-dependent dose enhancement effects. At extremely high fluence, saturation phenomena in the excess base current are evident for ionizing sources, but there is no apparent saturation for similar fluence of atomic-displacement sources. Such saturation phenomena are also evident in experiments combining mixed-mode electrical stress and medium-energy proton irradiation, as shown in Chapter 3. An analysis of the post-irradiation base current ideality factors suggest that in both 1^{st}- and 3^{rd}-generation HBTs, the observed excess base current is dominated by surface SRH recombination for 1.2 MeV ^{60}Co gammas and 10 keV x-rays up to 100 Mrad(SiO_2). Conversely, for 24 GeV protons and 1 MeV neutrons, the post-irradiation base current ideality factors suggest that band-to-band tunneling may play a significant role in the observed excess base current for 3^{rd}-generation HBTs but not for 1^{st}-generation HBTs. These nuances are the result of the properties of the BE spacer and STI oxides as well as the doping profiles, as discussed in Chapter 4.

10.2 Single-Event Effects

Although SiGe HBTs are remarkably tolerant atomic displacement and ionization, they are extremely vulnerable to a myriad of single-event effects at the transistor and circuit level, as demonstrated in Chapters 5-9. The results of single-photon pulsed laser irradiation on 1^{st}-generation HBT digital logic demonstrate the efficacy of circuit-level RHBD techniques in potentially reducing the on-orbit event rate, as evidenced by a comparison the average error length, single-bit error percentage, and the average BIE, as presented in Chapter 5. Furthermore, the pulsed laser irradiation technique has been demonstrated to be an invaluable tool in identifying the location-dependent SEE sensitivity in HBT digital logic, which can then be used to refine RHBD approaches by focusing on hardening only the most sensitive elements of the circuit.

The dependence of the total-dose and single-event response of 3^{rd}-generation HBTs and HBT digital logic on temperature has been investigated in Chapter 6. At cryogenic

temperatures, hole immobilization in the bulk SiO_2 suppresses the creation of Si/SiO_2 interface traps, which results in a reduction in the radiation-induced excess base current. Conversely, in the bulk Si regions, both the electron and hole mobilities increase as the temperature is reduced, which increases the drift-dominated charge collection volume and the collector-collected charge. To this end, a 300% increase in the proton-induced cross section at 77 K has been observed for HBT digital logic, as presented in Chapter 6. At room temperature, the proton-induced cross section is several orders of magnitude lower than the heavy-ion cross section as a result of the low LET and yield of the secondary products generated by proton-Si reactions. This result strongly suggests that as the temperature is reduced in a heavy-ion broadbeam environment, there will be even larger increases in both the bit-error and error-event cross sections, which should result in significant increases in the heavy-ion-induced upset rate.

To facilitate the mitigation of single-event effects in SiGe HBTs, a technique for layout-based modification of the transistor was introduced in Chapter 7. The technique is based on the inclusion of an alternate phosphorus-doped region in the transistor, which is known as the n-ring. Therefore, the substrate-to-n-ring junction is designed to compete with the substrate-to-sub-collector junction for unrecombined electrons following a ion strike. Several variations of this approach were evaluated, and heavy-ion microbeam and 3-D TCAD simulations were used to demonstrate that the placement of the n-ring outside the DT and the simultaneous reduction of the area enclosed within the DT, offered the most mitigation. Unfortunately, this technique is only capable of reducing the collector-collected charge for heavy ions that are impingent outside the DT but offers no protection for heavy ions impingent inside the DT. The transistor-level collector-collected charge obtained from time integral of the corresponding current transient, which was obtained using two-photon pulsed laser irradiation as presented in Chapter 8, is in agreement with the heavy-ion-induced collector-collected charge.

When implemented into an unhardened 16-bit shift register, transistors equipped with the external n-ring provide some reduction in the error-event cross section and the on-orbit event rate. Although the magnitude of these reductions is too small for the technique

to be considered as a standalone technique for SEE mitigation in HBT digital logic, the transistor-level layout-based RHBD approach should definitely be considered as a viable tool to be used in concert with others toward achieving a non-TMR single-event immune RHBD solution.

10.3 Recommendations

Based on the material covered in this dissertation, several recommendations can be made regarding the hardness assurance testing of SiGe HBTs and radiation hardening by design approaches for HBTs and HBT digital logic.

- 10 keV x-rays are typically the cheapest ionization source available, and depending on the dose rate, are capable of accurately replicating both the 63 MeV proton and 1.2 MeV ^{60}Co gamma response. Therefore, investigations into the effects of atomic displacement and ionization on bulk SiGe HBTs to be used in space-based electronic components should be performed using 10 keV x-rays, unless other circumstances warrant the use of other radiation sources.

- Further evaluation of atomic displacement and ionization effects in SiGe HBTs should focus in more detail on the impact of transistor and circuit bias during irradiation by monitoring bias currents and voltages while fluence is being accumulated [385].

- The impact of extreme high- and low-energy proton fluence on the *ac*-performance characteristics should be evaluated, since under these conditions there is clear evidence of atomic displacement effects, as evidenced by the damage factor calculations presented in Chapter 4.

- Heavy-ion broadbeam irradiation should be performed at cryogenic temperatures.

- The effect of combining transistor- and circuit-level RHBD techniques on SEE mitigation for HBT digital logic should be investigated.

- New transistor-level layout-based RHBD techniques should focus on reducing the peak magnitude of the heavy-ion-induced current transients for heavy ion strikes inside the

DT, even at a modest performance penalty, as demonstrated for the "inverse-cascode" HBT described in [386].

- The impact of variations in the area of the base-to-collector and substrate-to-sub-collector junctions should be investigated to determine their relative contributions to the observed heavy-ion-induced current transients.

- New circuit-level RHBD designs should always seek to increase the critical charge without increasing the total transistor count or the area enclosed within the DT.

- Accurate mixed-mode TCAD should be performed to isolate the impact of the prompt and delayed transients on the observed response as a function of circuit bias, speed, and radiation environment.

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VITA

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Akil has interned for four summers at the IBM T.J. Watson Research Center working on a variety of projects ranging from laser spike annealing of SiGe HBTs to high resolution metal lift off characterization and deep Si reactive ion etch techniques.

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